

A Low Power 1MHz Fully Programmable Frequency Divider in 45nm CMOS Technology

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Abstract

A low power 1MHz Full programmable frequency divider in 45-nm CMOS process is presented in this paper. The divide ratio can be varied from 2400 to 2431 in a step size of 1. The divider consists of a divide-by-2 circuit, divide-by-2/3 prescaler, divide-by-32/33 prescaler, a programmable pulse-swallow counter. The post simulation results demonstrate that the divider can operate with the input frequency ranging from 2.46GHz-2.541GHz. Measured results show that programmable divider consuming only 613.39 μ W at 1V power supply. The programmable frequency divider is design and simulated on Tanner EDA Tool using 45nm CMOS process technology with supply voltage 1 V.

Keywords: Phase locked loop (PLL), True Single Phase Clocked (TSPC), Voltage control oscillator (VCO), Phase frequency detector (PFD, Tanner Tool).

I. INTRODUCTION

The Programmable frequency divider consists of a Dual-Modulus Prescaler (DMP), a Programmable (P) Counter and a Swallow (S) Counter. The Dual-Modulus Prescaler is based on both synchronous and asynchronous divider which scales the input frequency to a lower frequency to ease the complexity of asynchronous resettable modulo-P and modulo-S counters. In this technique, S input pulses are swallowed in the preceding arrangement such that the output period becomes longer by S reference periods. In the initial state, the Modulus Control (MC) signal remains at logic '0' and allows the Dual Modulus Prescaler (DMP) to operate in the divide-by-($N+1$) mode and the programmable P-counter and swallow S-counter are loaded to their initial states. Since $P > S$, the S-counter reaches the final state earlier than P-counter and the end-of-count logic of the S-counter changes the MC to logic '1' allowing the DMP to switch to divide-by- N mode where the P-counter counts the remaining ($P-S$) input periods of ' N '. Thus the total division ratio is given by

$$f_{out} = ((N+1) \cdot S + N \cdot (P-S)) \cdot f_{in} = (NP+S) \cdot f_{in}. \quad (1)$$

From the circuit topology view point, prescalers and presettable counters are often implemented using different logic families, owing to their different speed specifications and a level shifter is required after the Dual Modulus Prescaler (DMP) to compensate different voltage rails. The basic programmable frequency divider architecture is shown in figure 1^[1]. The programmable frequency divider architecture consists of dual modulus 32/33 prescaler, 7-bit programmable counter, 5-bit swallow counter. Divide by 32/33 prescaler consists of one 2/3 prescaler unit, combination of NAND and NOR gates and four stages of toggled divide-by-2 units using DFFs. When the control signal MC is logically high, the 32/33 prescaler functions as divide-by-32 unit and the control logic signal MC to the 2/3 prescaler goes logically high allowing it to operate in divide-by-2 mode for the whole 32 clock cycles. When control logic signal MOD is logically low, the 32/33 prescaler unit functions as divide-by-33 unit during.

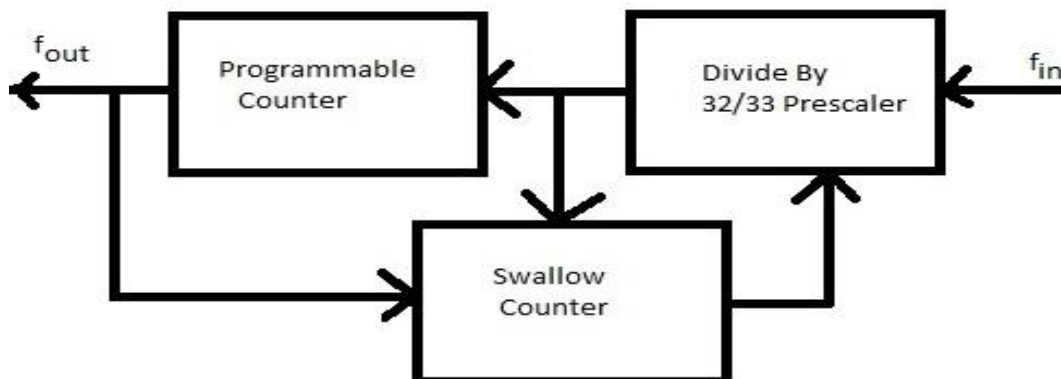


Fig. 1: Programmable Frequency Divider Architecture

II. DIVIDE BY 32/33 PRESCALER

A. Divide By 32/33 Prescaler

Figure 2 shows the topology of a general 32/33 prescaler [2]. When the control signal MC is logically high, the 32/33 prescaler function as divide-by-32 unit and the control logic signal MC to the 2/3 prescaler goes logically high allowing it to operate in divide-by-2 mode for the whole 32 clock cycles. When control logic signal MC is logically low, the 32/33 prescaler unit function as divide-by- 33 unit during which 2/3 prescaler operates in divide-by-3 mode for 3 input clock cycles and in divide-by-2 mode for 30 input clock cycles [2].

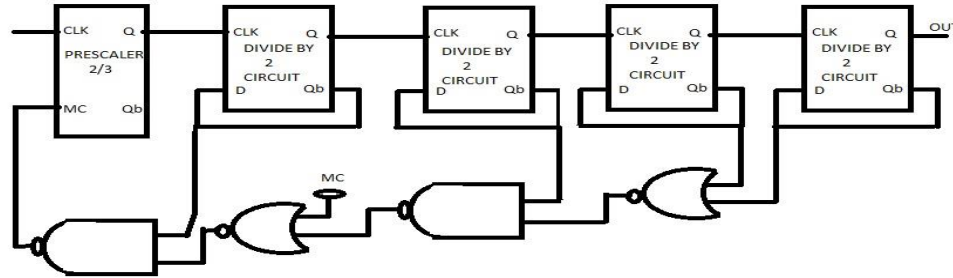


Fig. 2: Divide By 32/33 Prescaler

1) Divide-By-32 operation (MOD= '1')

When the control signal MOD is '1', the output of NOR2 always remains at logic '0' and forces the output of NAND2 to logic '1' irrespective of data on Qb1. Since MC is always equal to logic '1', the Design of prescaler remains in divide-by-2. Thus the 32/33 prescaler acts as divide-by-32 circuit. Since control logic signal MC is logically high, DFF1 in the 2/3 prescaler is completely turned-off for the entire 32 input clock cycles. The 32/33 prescaler consists of both the synchronous and asynchronous (toggle divide-by-2) circuits and thus the power and speed is traded-off as discussed in the design of digital counters earlier. If we denote the synchronous 2/3 prescaler as M/M+1 and the four asynchronous dividers whose division ratio equal to 16 by 'AD', the division ratio in this mode (MOD= '1') is given by

$$f_{32} = (AD - \overline{MOD}) \times M + \overline{MOD} \times (M + 1) = 32 \quad (2)$$

2) Divide-By-33 operation (MOD= '0')

The dual-modulus 32/33 prescaler operates as divide-by-33 when MOD='0'. By using the combination of logic NOR and NAND gates, the asynchronous divide-by-16 counter is made to count an extra input clock. The control signal MC is given by

$$MC = \overline{Q_{b4}} + \overline{Q_{b3}} + \overline{Q_{b2}} + \overline{Q_{b1}} + MOD$$

In the initial state, 2/3 prescaler will be in divide-by-2 mode (MC= '1') and the asynchronous divide-by16 starts counting the output pulses of 2/3 prescaler from "0000" to "1111". When the asynchronous counter value reaches "1110", the logic signal MC goes low (MC='0') and the prescaler operates in divide-by-3 mode, where the asynchronous counter counts an extra input clock pulse. During this operation, the 2/3 prescaler operates in divide-by-2 mode for 30 input clock cycles and for the remaining 3 input clock cycles; it operates in divide-by-3 mode. The division of the 32/33 prescaler in this mode is given by

$$f_{32} = (AD - MOD) \times M + MOD \times (M + 1) = 33 \quad (3)$$

where AD=16, MOD='0' and M='2'.

B. Divide By 2/3 Prescaler

The TSPC divide-by-2 unit has the merit of high operating frequency compared with the traditional TSPC divide-by 2 unit. Since the divide-by-2/3 unit consists of two toggle DFFs and additional logic gates, one way to effectively reduce the delay and power consumption is to integrate the logic gates to the divide-by-2/3 unit [2]. Divide-by-2/3 counter design is given in Figure 3 consists of two TSPC-based FFs and two logic gates, an OR gate and an AND gate. When the divide control signal is low, the OR gate (merged into output of FF1 stage) is disabled. This corresponds to a divide-by-3 function. Note that state 10 is a forbidden state. If, somehow, the circuit enters this state, the next state will go back to a valid state, 11, automatically. When high is the output of FF1 will be disabled and FF2 alone performs divide-by-2 function. The control logic signal MC selects the divide-by-2 or divide-by-3 mode. When MC is logically high DFF1 will disconnected from the power supply and DFF2 alone work to form the divide-by-2 operation. When the control signal MC goes low than both flip-flops combine give the divide-by-3 operation. Operating frequency is directly related to the supply voltage.

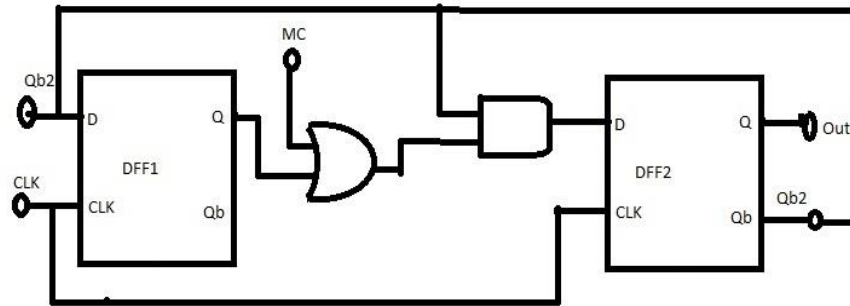


Fig. 3: Divide By 2/3 Prescaler

The Divide by 2/3 prescaler is implemented with True Signal Phase Clock (TSPC) logic. When control logic signal ‘MC’ goes high, the output of OR gate is always equal to logic ‘1’ and the output of AND gate is always equal to the inverted output of DFF2 (Q2) such that the prescaler operates in the divide-by-2 mode as shown in Fig. 3. When control logic signal ‘MC’ goes low, the output of OR gate is always equal to ‘Q1’, such that prescaler operates in the divide-by-3 mode as shown in Figure 3. The output of the synchronous 2/3 prescaler is given by

$$f_{out} = \overline{MC} \cdot (f_{in}/3) + MC \cdot (f_{in}/2) \quad (4)$$

C. Divide By 2 Circuit

The divide by 2 circuit is realized in the TSPC logic as shown in figure 4^[5]. The salient feature of the TSPC clocking technique is that there only one clock signal needed to trigger the flip-flop and no extra clock phase is required. This technique is mainly used in dynamic CMOS circuits and helps to simplify the design. The circuit consists of three parts. The first part is gated inverter that consists of Mp1, Mp2, and Mn1, which passes the divider output to the following stage when the clock is low. The second part is latch stage that consists of Mp2, Mp3, Mn2, Mn3, Mn4, and Mn5. This circuit will be activated and store the output of the gate inverter when clock is high. The PMOS transistor Mp1 and Mp2 are used to pre-charge the internal nodes to increase the speed of the circuit.

The output of the flip-flop is directly connected back to the D-input to obtain the divided by 2 function because the TSPC circuit can complicity isolated the sense and latch stage at different phase of the clock signal. The static power of the circuit is zero because path from the supply to ground exist and it only consumes dynamic power.

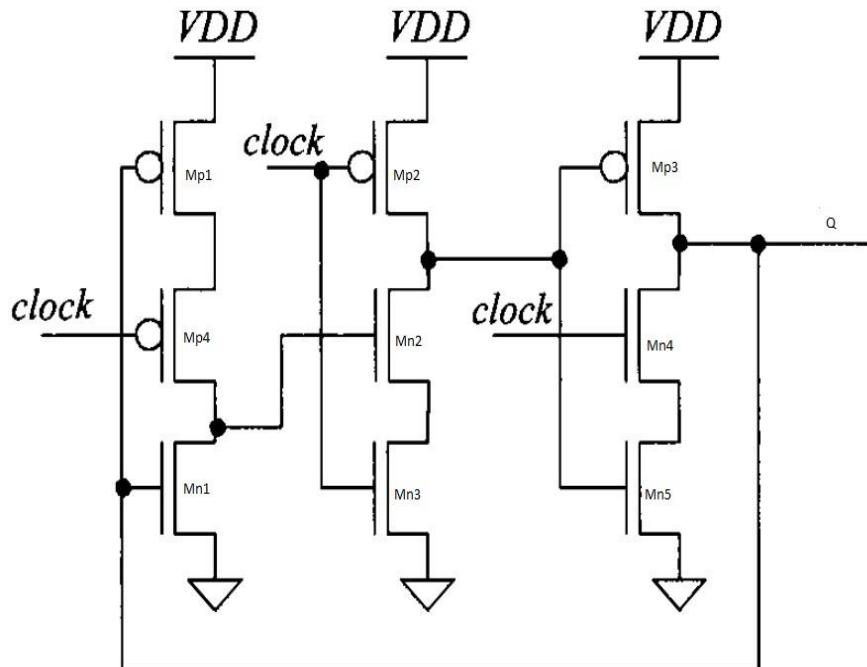


Fig. 4: Divide By 2 circuit using TSPC logi

D. Simulation Result of Divide By 2 Circuit

The transient analysis of divide by 2 circuit is shown in figure 5. The CLK frequency is 2.4GHz and Q is the divide by 2 output frequency which is 1.2GHz.

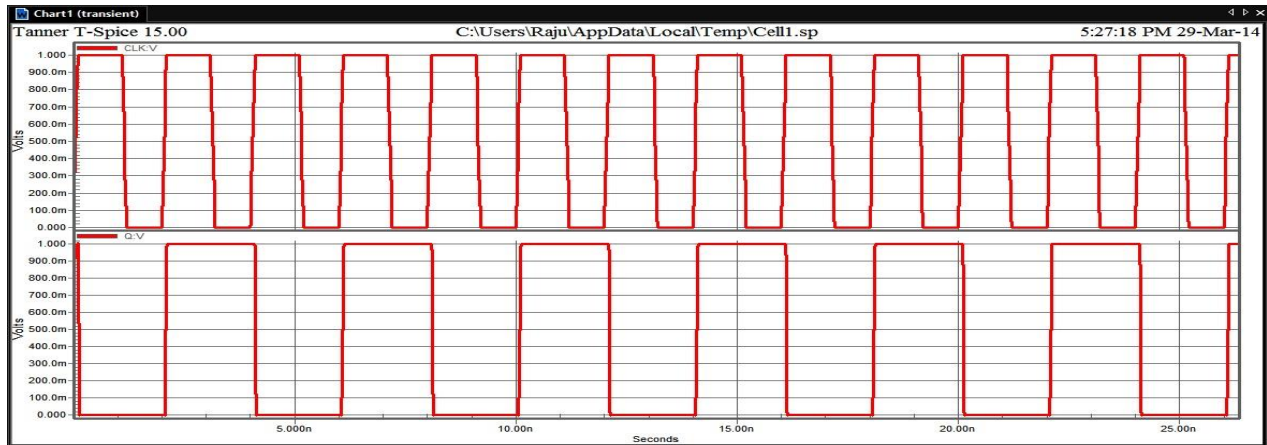


Fig. 5: Divided By 2 output

E. Simulation Result of 2/3 Prescaler

The figure 6 and 7 shows the transient analysis of the 2/3 prescaler respectively. The input CLK frequency is 2.4 GHz. When MC=1 its output is divided by 2, which is 1.2GHz and power dissipation is 59.15 μ W during divide by 2 operation. The figure 6 divide by 2 operation.

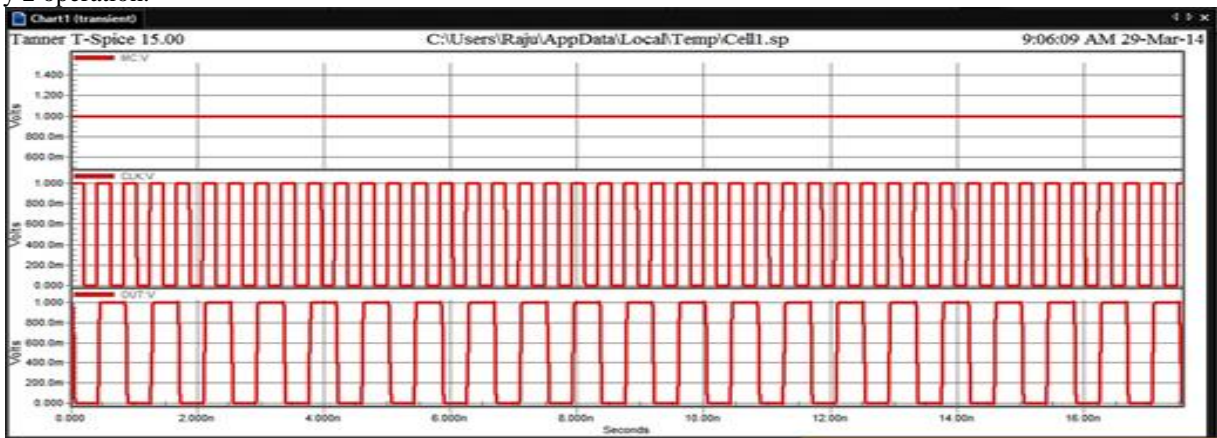


Fig. 6: Divided By 2 output of Prescaler

When MC=0 its output is divided by 3, which is 801.28MHz and power dissipation is 61.47 μ W during divide by 2 operation. The figure 7 divide by 3 operation.

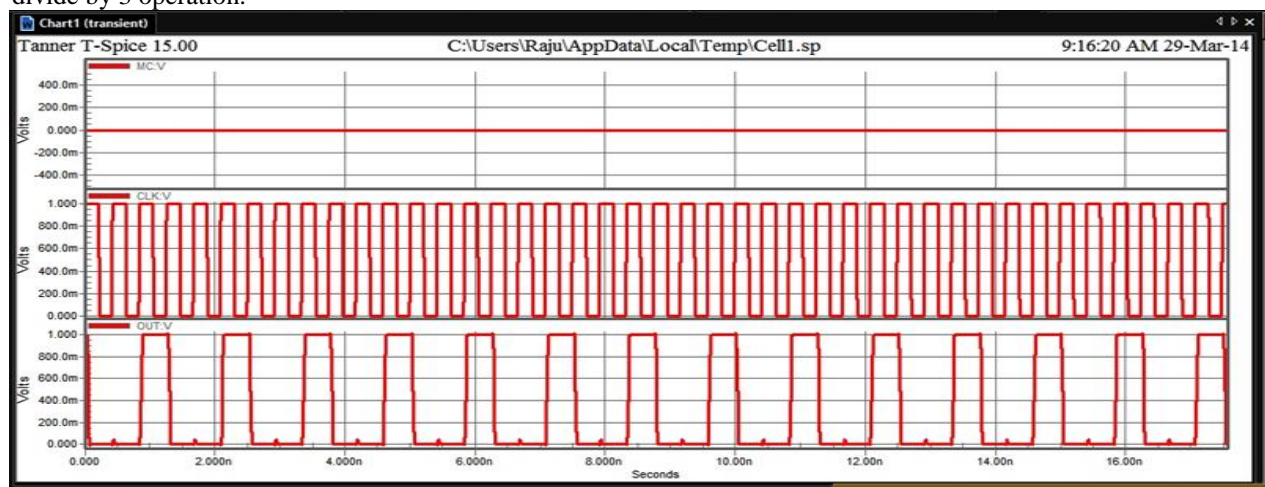


Fig. 7: Divided By 3 output of Prescale

F. Simulation Result of 32/33 Prescaler

The figure 8 and 9 shows the transient analysis of the 32/33 prescaler respectively. The input CLK frequency is 2.4GHz. When MC=1 its output is divided by 32, which is 75.11MHz and power dissipation is 85.62 μ W during divide by 32 operation.

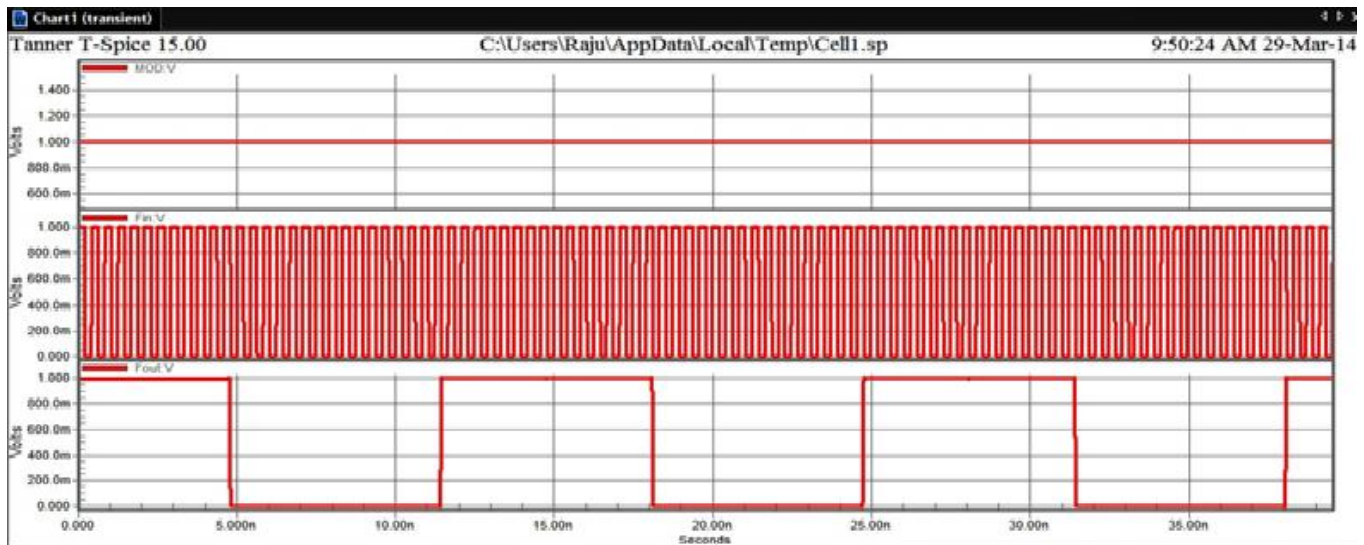


Fig. 8: Divided By 32 output of Prescaler

When MC=0 its output is divided by 33, which is 72.72MHz and power dissipation is 86.49μW during divide by 33 operation.

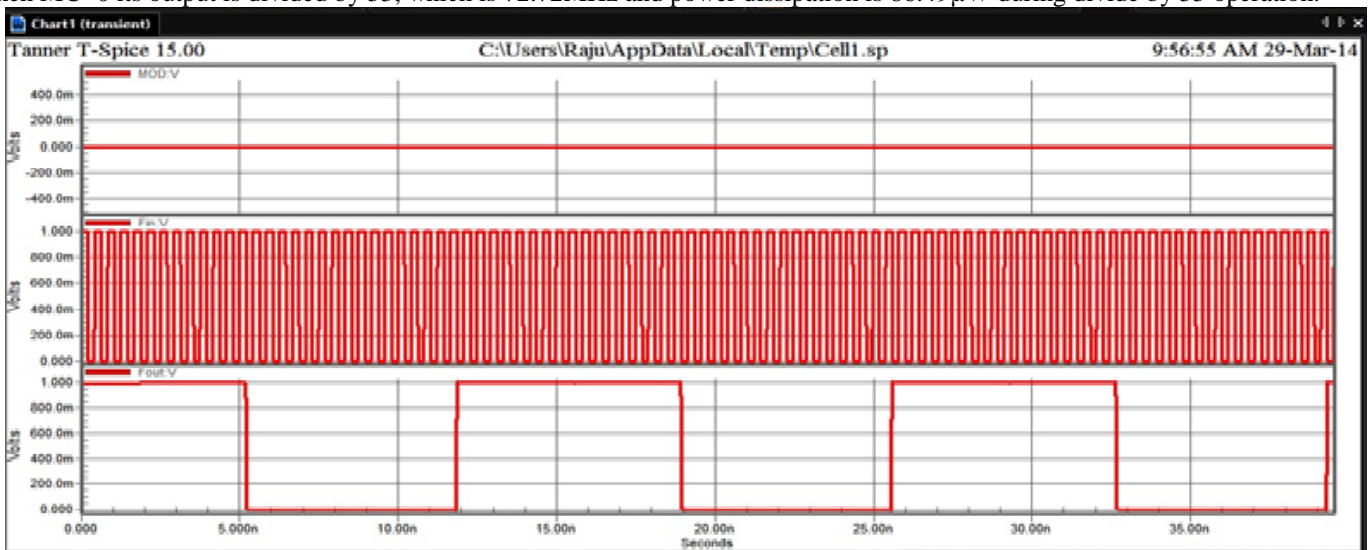


Fig. 9: Divided By 33 output of Prescaler

III. P-S COUNTER

For PLL Frequency Synthesizers operating in the 2.4 GHz ISM band [4]-[3], with a resolution of 1MHz and division ratios of 2400-2484 can be achieved with a 32/33 prescaler, a 7 bit P-counter and a 5 bit S-counter. Fig.1 shows the fully programmable divider with a division ratio from 2400 to 2484 in steps of 1. In this design, only bits P1, P2 and P3 of the P-counter are used programming and the bits P4, P5, P6 and P7 are fixed at '1', '0', '0' and '1' respectively to have P-values between 74-77. Here all the bits of S-counter are used for programming. The P and S counter's programmable value for the division ratios between 2400-2484 is shown in Table 6.1. This chapter briefly discusses the design of a fully programmable 1MHz resolution divider based on pulse swallow divider topology.

The Frequency Division ratio (FD) of the multi-band divider in this mode is given by

$$FD = N \times P - S \quad (5)$$

Where FD = frequency division ratio, N = Modulus value, P = P-Counter value, S = S-Counter value.

Hence from table 1 it can be seen than the by changing the programming values of the Programmable P-Counter and Swallow Counter different frequency division ratio is achieved for frequency synthesizer.

Table. 1: Programmable values of the Programmable Counters

Frequency division ratio	Prescaler (N/N+1)	Programmable counter (P)	Swallow counter(S)
2400-2431	N=32	P=75	S=0-31

2432-2463	N=32	P=76	S=0-31
2464-2484	N=32	P=77	S=0-20

A. Programmable Counter

The 32/33 prescaler scales the input 2.4 GHz signal by a value of 32 or 33 such that the P and S counters will be working in the frequency range of 72 - 78 MHz in order to obtain the 1 MHz frequency output. The design requirements of the P-counter in the design of 2.4 GHz fully programmable divider are as follows:

- Operate at frequencies of up to several 100 MHz with low power consumption.
- Able to program the desired P values from 74 to 77.
- To generate full-swing output, which is fed to the phase frequency detector block

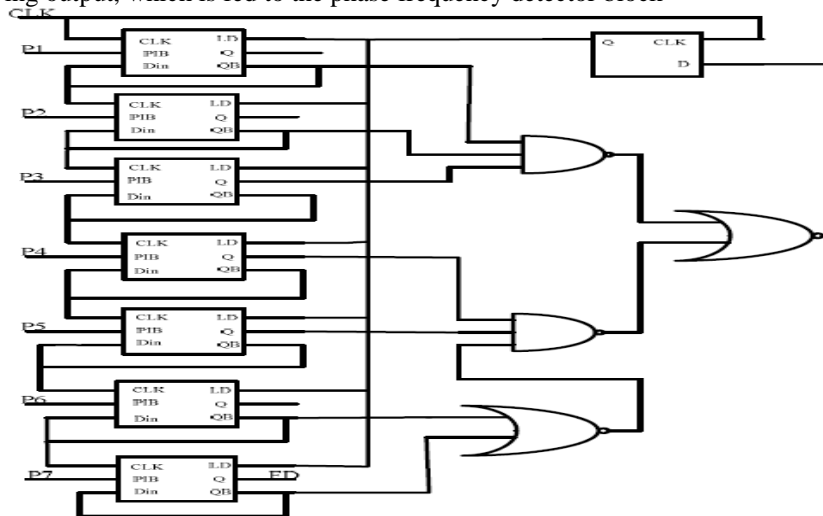


Fig. 10: A 7-bit programmable P-Counter

The Programmable P-Counter used in the design of the fully programmable divider is a 7-bit asynchronous down counter as shown in Fig.10^[4]. The P-counter is designed with 7 reloadable TSPC D Flip-Flops (DFF) and an End-Of- Count (EOC) detector which has reload circuit in it ^[3]. Since the counter is asynchronous and based on the ring topology, the complementary output of the first DFF is fed as clock to the input of next flip-flop. In the initial state, all the reloadable FF's are loaded by the programmable pins P1-P7. As the counter is triggered by the output of the prescaler, the P-counter starts down counting till the state "0000000" is reached. Once this state is detected by the EOC logic circuit, the load (LD) signal goes high to reset all loadable FF's to the initial state.

B. Swallow S-Counter

The fully programmable divider also consists of a 5-bit swallow S-Counter whose design requirements are as follows:

- To operate at frequencies of up to several 100 MHz with low power consumption.
- To load the programmable S values from 0 to 31 in steps of one and stop the operation when S counting is finished.
- To generate a full-swing output, this is given as feedback signal to phase frequency detector block

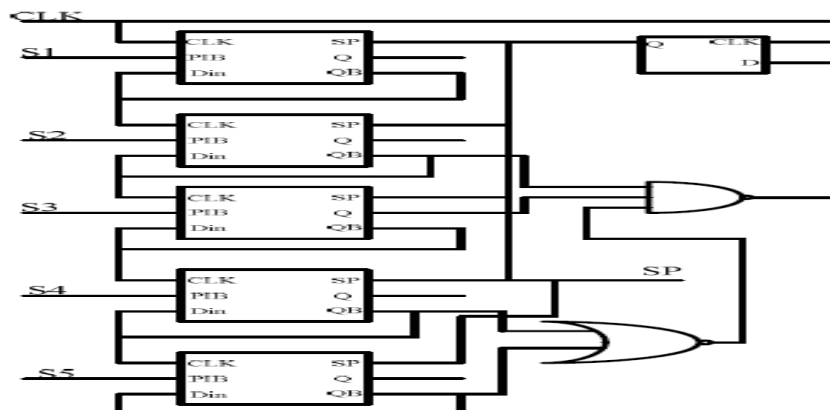


Figure. 11 A 5-bit Swallow S-Counter

The Swallow S-Counter used in the design of the fully programmable divider is a 5-bit asynchronous down counter as shown in Fig.11. The S-counter is designed with 5 reloadable TSPC D flip-flops and an End-Of- Count (EOC) detector with the reload circuit [1]. Since the counter is asynchronous and based on the ring topology, the complementary output of the first DFF is fed as clock to the input of next flip-flop. In the initial state, all the reloadable FF's are loaded by the programmable value set by pins S1-S5. In the S-counter all states from 0-31 are usable and adjustable in steps of 1 to obtain a resolution of 1MHz. Once the counter is triggered by the output of the prescaler, the S-counter starts down counting till the final state is reached, which is detected by the EOC logic circuit and the stop (SP) signal goes high until the P-counter finishes it's counting. Since the value of 'P' is always greater than value of 'S' in pulse-swallow divider, the S-counter remains idle for a period of $(P-S)*N$ clock cycles.

IV. SIMULATION RESULT OF PROGRAMMABLE FREQUENCY DIVIDER

The simulations of the fully Programmable Frequency Divider with 1MHz resolution are performed using Tanner EDA tool for a 45 nm CMOS process. Fig.13 shows the simulation results of the fully programmable divider. The simulations are performed by giving a 2.4GHz square wave signal with amplitude of 0.5V (peak) to the prescaler. Here the programmability of the divider is set to 2400 and the results indicate that the output of the fully programmable divider is 1MHz. Figure 12 shows Schematic view of Programmable Frequency Divider.

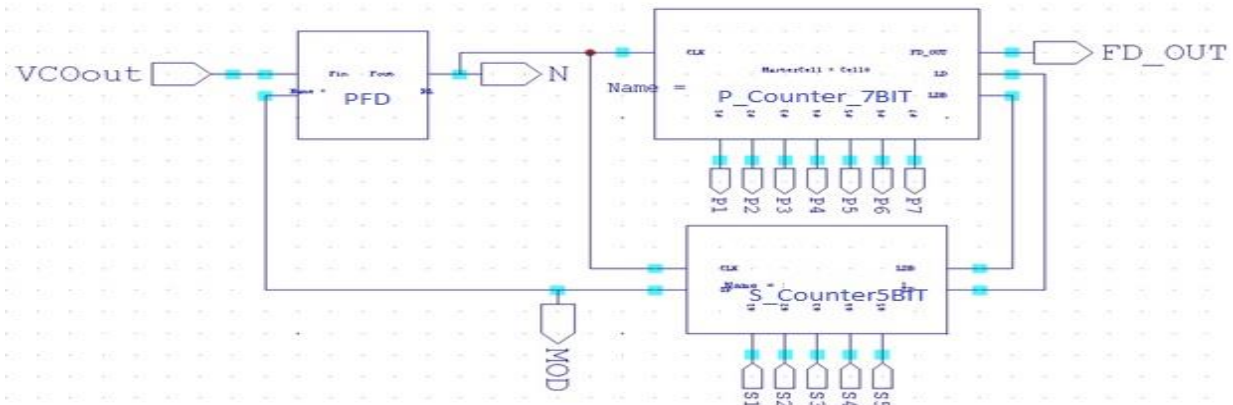


Fig. 12: Schematic view of Programmable Frequency Divider

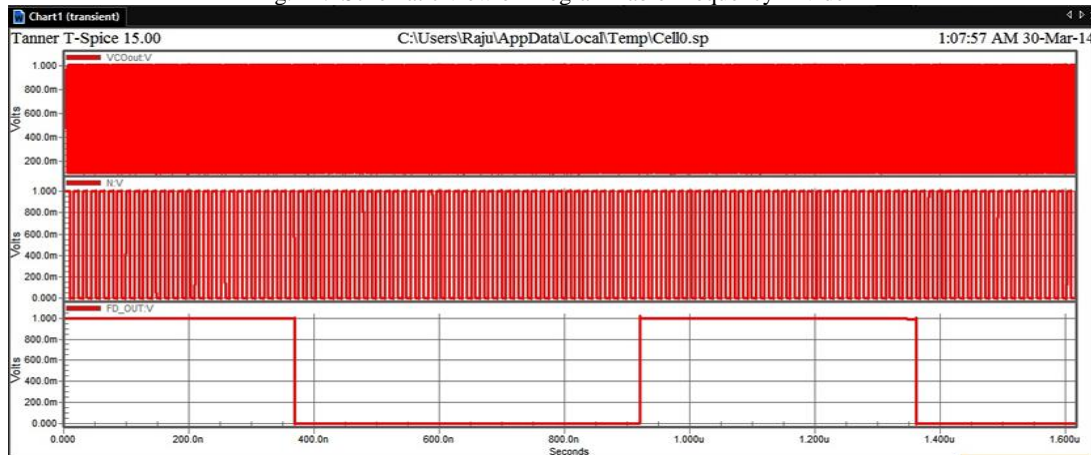


Figure 13 Simulation Result of Programmable Frequency Divider

Table. 2.: Frequency Divider Performance Summary

Specification		Simulation Result
Technology		45nm
Supply voltage		1V
Frequency Band		2.46GHz-2.541GHz
Ref. Frequency		1MHz
Power Dissipation	2 Prescaler	59.15μW/
	3 Prescaler	61.47μW
	32 Prescaler	85.62μW/
	33 Prescaler	86.42μW
	Frequency Divider	613.39μW

V. CONCLUSION

This paper presents a programmable frequency divider designed in 45-nm CMOS process with divide ratio varied from 2400 to 2431 in a step of 1. The post simulation results show that the divider can work properly with the input frequency from 2.44GHz to 2.54 GHz while the power consumption is 613.39 μ W at supply voltage of 1V. The DFF in the prescaler is controlled by the mode controlling signal and powered off in the idle state, the DFFs in the program counter and swallow counter are shared, and thus power consumption is reduced. The experimental results show large power reduction is achieved by the proposed divider. We can conclude that the proposed divider is well suitable for low power design.

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