Design High Speed Conventional D Flip-Flop using 32nm CMOS Technology

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Abstract

A Delay (D) flip-flop is an edge triggering device. A high speed, low power consumption, positive edge triggered conventional Delay (D) flip-flop can be designed for increasing the speed of counter in Phase locked loop, using 32nm CMOS technology. The conventional D flip-flop has higher operating frequencies but it features static power dissipation. The designed counter can be used in the divider chip of the phase locked loop. A divide counter is required in the feedback loop to increase the VCO frequency above the input reference frequency. The propose circuit will be faster than conventional circuit as it will be a fast reset operation. The circuit will be consuming less power as it prevents short circuit power consumption. The circuit operates at low voltage power supply.

Keywords: Phase Locked Loop (PLL), D-ff, Phase Frequency Detector (PFD) and Voltage Control Oscillator (VCO)

I. INTRODUCTION

PLL is an important analog circuit used in various communication applications such as frequency synthesizer, radio computer, clock generation microprocessors etc. The D flip-flop is an important part of the modern digital circuit. Flip flop can be regarded as a basic memory cell because it stores the value along the data line with the vantage of the output being synchronized to a clock. Flip flops are used as registers. D flip flop is a best choice for storage registers. The many logic synthesis tool use only D flip flop or D latch. The working of D flip flop is similar to the D latch except that the output of D Flip Flop takes the state of the D input at the moment of a positive edge at the clock pin (or negative edge if the clock input is active low) and delays it by one clock cycle. That's why, it is commonly known as a delayed flip flop.

The proposed work would be a brief overview of Phase Locked Loop (PLL). A phase locked loop with an excellent performance widely studies in recent years. Frequency divider and PFD are indispensable modules of PLL, which uses conventional D flip-flop as an integral component. Edge Triggered D flip flops are often implemented in integrated high speed operations using dynamic logic. This means that the digital output is stored in the parasitic device capacitance while the device is not transitioning. This design of dynamic flip flops also enables simple resetting since the reset operation can be performed by simply discharging one or more internal nodes. The conventional D flip-flop which uses E-TSPC (True signal phase clock) logic has higher operating frequencies but it features static power dissipation. However, this causes a small increase in power dissipation, since at the frequencies of interest dynamic power consumption is dominant. In the proposed circuit dynamic power consumption was reduced by lowering internal switching and speed is increased by shortening input to the output path.

II. PHASE LOCKED LOOP (PLL)

Phase locked loop is generally used in wireless communication and data recovery circuits. At present, for the above mentioned application a low voltage, low area and high performance integrated circuits are used which complicates the execution of such type of integrated circuit.

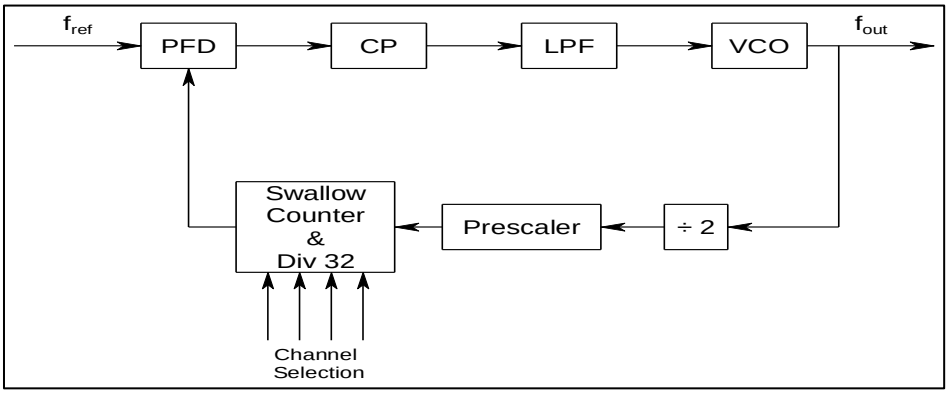

Fig. 1: Block diagram of PLL

A PLL is a control system that generates a signal that has a fixed relation to the stage of a "reference" signal. A phase-locked loop circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is coupled to the character in both frequency and phase. Phase locked loops are built of a detector, charge pump, low pass filter, voltage-controlled oscillator (VCO) and frequency divider placed in a negative feedback closed-loop configuration. A phase detector compares two input signals and produces an error signal which is proportional to their phase difference. The error signal is then low-pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, creating a negative feedback loop. If the output frequency drifts, the error signal will increase, driving the VCO frequency in the opposite direction so as to reduce the error. Thus the output is locked to the frequency of the other input.

A. Phase Frequency Detector:

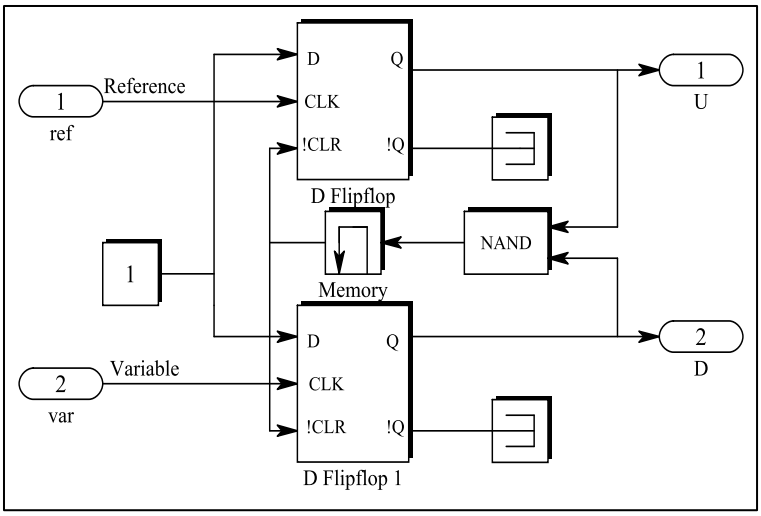

Fig. 2: Block diagram of PFD

A phase frequency detector (PFD), is a device which compares the phase of two input signals and provides a signal in the form of phase error. It accepts two inputs which correspond to two different input signals, usually one from a voltage-controlled oscillator (VCO) and the other is a reference source. It has two outputs which instruct subsequent circuitry on how to adjust to lock onto the phase. A charge pump circuit is used to convert the digital signal from the phase frequency detector to an analog signal, the output of which is used to control the frequency of the voltage control oscillator. To form a phase-locked loop (PLL), the phase error output of PFD is fed to a charge pump and then to loop filter which integrates the signal to get a sharper and smoother signal so that the disturbances at the input of VCO get minimized. As can be ascertained from the following diagram, the D flip-flop is an integral part of pfd. Hence, to make the operation of PFD faster, a fast D flip-flop is required.

B. Frequency Divider:

Frequency divider divides the VCO frequency to generate a frequency which is compared with reference frequency. In the block diagram PLL, the prescaler and swallow counter together acts as a frequency divider. D flip flop is an integral part of both of them.

C. Voltage Controlled Oscillator:

A voltage-controlled oscillator or VCO is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency. Consequently, modulating signals applied to control input may cause frequency modulation (FM) or phase modulation (PM). A VCO may also be part of a phase-locked loop.

D. Low Pass Filter:

A low-pass filter is a filter that passes low-frequency signals. Attenuates signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies depending on specific filter design. It is sometimes called a high-cut filter, or treble cut filter in audio applications. A low-pass filter is the opposite of a high-pass filter. A band-pass filter is a combination of a low-pass and a high-pass.

Low-pass filters exist in many different forms, including electronic circuits, anti-aliasing filters for conditioning signals prior to the analog-to-digital conversion, digital filters for smoothing sets of data. Also for acoustic barriers, blurring of images, and so forth. The moving average operation used in areas such as finance is a particular kind of low-pass filter, and can be analyzed with the same signal processing techniques as are used for other low-pass filters. Low-pass filters provide a smoother form of a signal, removing the short-term fluctuations, and leaving the long-term trend. An optical filter can correctly be called a low-pass filter, but is conventionally called a long pass filter (low frequency is long wavelength), to avoid confusion.

III. RELATED WORK

From the rigorous review of related work and published literature, it is observed that many researchers have designed D flip-flop for phase locked loop (PLL) by applying different techniques like analog and digital simulation applying mathematical/logical relations. Researchers have undertaken different systems, processes or phenomena with regard to design and analyze performance of D flip-flop and attempted to find the unknown parameters. Since in the real world today VLSI is in very much in demand, from the careful study of reported work it is observed that very few researchers have taken a work for designing D flip-flop for phase locked loop (PLL) with 32nm CMOS technology.

A survey of D flip flop for PLL is presented by R H Talwekar in his paper. Both classical and modem approaches are discussed. He suggested that although the design of PLL is fairly well documented, more needs to be done to pinpoint the formal design of the D-PLL, the primary use of the PLL has been in more sophisticated communication systems, however with the rapid development of IC Technology, time is not far when PLL's will be used widely in consumer electronics. A high speed low power consumption positive edge triggered Delayed (D) flip-flop was designed for increasing the speed of counter in Phase locked loop, using 180 nm CMOS technology. The designed counter has been used in the divider chip of the phase locked loop. [1]

These D flip-flops are very useful, as they form the basis for shift register, which are an essential part of many electronic devices. The advantage of the D flip-flop over the D-type "transparent latch" is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. It put up by Yubtzuan Chen, Chih Ho Tu and Jein Wu an improved CMOS Phase/Frequency Detector (PFD) is presented. A high-speed low-power CMOS D-type master-slave flip-flop is proposed and adopted in the PFD. Higher speed and lower power operation are attributed to the reduced node capacitance. Charge-sharing phenomena are circumvented in the proposed PFD. The proposed PFD shows improvement in frequency sensitivity at high operating frequency. The proposed PFD is suitable for high-speed low-power operation. [2]

In this paper S. H. Yang design a new dynamic D flip-flop for high speed operation and low power consumption is presented aiming at glitch free operation. Here transistor merging technique has been employed to reduce the number of transistor and to secure reliable high speed operation. The flip-flop consists of only nine transistors based on the transistor merging technique, which is smaller than other alternatives. The fewer transistors in the flip-flop can achieve faster operation and lower power consumption. To evaluate the proposed flip-flop circuit, a dual-modulus divide by 128/129 prescaler has been designed and fabricated using 0.25μm CMOS technology. At the 2.5V supply voltage, the prescaler using the proposed dynamic D flip-flop can operate up to the frequency of 2.9GHz consuming 3.621mW and shows half the power delay product of Huang's circuits. [3]

Here author Won Hyo Lee and Jun Dong Cho introduce a high-speed and low power Phase-Frequency Detector (PFD) that is designed using modified TSPC (True Single-phase Clock) positive edge triggered D flip-flop. This PFD has a simpler structure with using only 19 transistors. The operation range of this PFD is over 1.2GHz without additional prescaler circuits. Furthermore, the PFD has a dead zone less than 0.0lns in the phase characteristics and has low phase sensitivity errors. The phase and frequency error detection range is not limited as in the case of the p-type and n-type PFD. Also the PFD is independent from the duty cycle of input signals. A new charge-pump circuit is presented that is designed using a charge-amplifier. A stand by current enhances the speed of charge - pump and removes the charge - sharing which causes a phase noise in the charge - pump PLL. Also, the effects of clock feed -through are reduced by separating the output stage from UP and down signal. The simulation results base on a third - order PLL are presented to verify the lock - in process with the proposed PFD and Charge - pump circuits. The PFD and charge - pump circuits are designed using 0.8 μm CMOS technology with 5V supply voltage. [4]

The survey of a D flip-flops for low power and high performance is demonstrated in this paper with a low supply voltage. The flip-flop has an increased current level so that to ensure the more loading capacity, compared to standard CMOS circuits which operating at low supply voltages. The delay of the static d flip-flop presented is less than 16% compared to conventional CMOS flip-flops. The design described here is simulated using Hspice and is valid for PTM 32nm process. The newly designed high speed and low-power flip-flop can be used for any digital application. We compare the two different flip flop circuits contain 10 transistors and 12 transistors. Basic features on different flip-flops evaluated based on timing characteristics, and power consumption. In this paper we propose a new system which comparatively reduce the number of transistor which will improve the reduction in clocking power and the overall power consumption. [5]

Low-power high-speed programmable dual modulus divider architecture is presented by Mohd S. Sulaiman and Nasserullah khan. The circuit's three building blocks: prescaler, 2- and 5-bit programmable dividers; were designed using high-performance single-phase clocking latch up circuits rather than the conventional latch up circuits widely used in digital systems. The dividers operate based on the modulus control and parallel loading concepts, capable of operating within the division ratio of 32 - 127. We have presented a dual-modulus divider with extremely low power consumption, designed in a 0.18μm CMOS process. The maximum operating frequency is 2.4 GHz with a 1.8-V supply and a power of only 2.26 mW. The programmable dual-modulus divider is intended for wireless applications, and when used with a low-power sigma-delta modulator, the resulting circuits are a very good candidate for modem wireless communication applications requiring high-performance and low-power circuits. Advances in CMOS technology and the use of advanced circuit architecture let us expect a significant reduction in power and increase in speed. [6]

Phase locked loop (PLL) is a main block in many applications such as wireless communication systems, digital circuits and sensors receivers. It is a clock or carrier generator. This application needs low power blocks to have long life battery. Phase

frequency detector (PFD) is one of the PLL blocks. The main concept of PFD is comparing two input frequencies in terms of both phase and frequency. This paper presents a new PFD design. This paper presents a new PFD design. Falling edge PFD (FE-PFD) is implemented using silterra 0.18µm CMOS process. It is composed of 12 transistors and preserves the main functionality of a conventional PFD. A charge pump design is presented. It is compatible with the characteristics of the proposed PFD and implemented with the same technology. They are tested in a PLL system. This paper was published by Nasreen M. H. Ismail and Masuri Othman. [7]

A high performance 32nm logic technology with 2nd generation high-k + metal gate transistors is presented. It is to be introduced by P. Packan, S. Akbar and others. Record NMOS and PMOS drive currents are reported, along with the tightest contacted gate pitch for a 32nm or 28nm technology. Variation for the 32nm technology was shown to be the same as the 45nm technology. Excellent Vcc min and the highest reported SRAM array density for 32nm or 28nm technology was reported. Fully functional 32nm processors using this technology were demonstrated in systems in Jan 2009 and are on track for volume production in 2H 2009. This 32nm technology maintains the historical scaling trends of both area and performance and continues Moore's law. [8]

IV. PROPOSED WORK

The proposed study will be to design, the conventional positive edge triggered D- flip flop in a 32nm CMOS technology. Also, some work done thereafter on this, but that is not sufficient so we are designing a new D-flip flop. By using this technique the required percentage of power consumption is low and also the speed of performing the procedure is high.

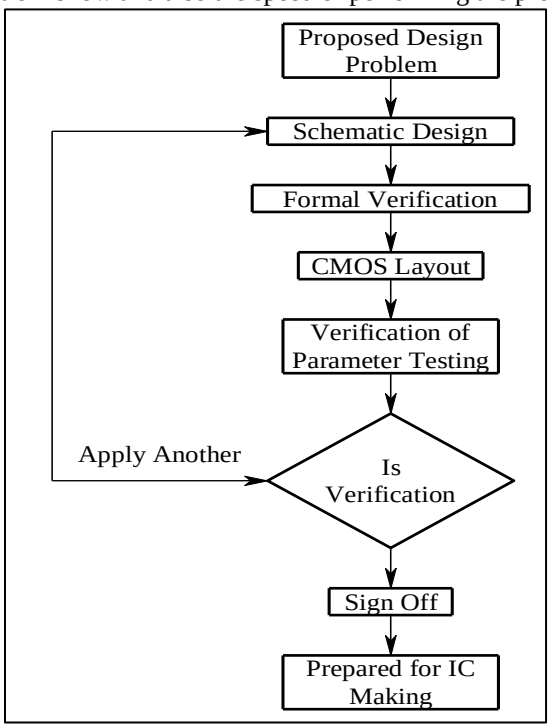

Fig. 3: Flow Chart of Proposed Work

For performing this project the different methodology and techniques can be used for research. The MICROWIND3.1 programs allow to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND 3.1 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices).

V. DESIGN IMPLEMENTATION

Here we design conventional D flip-flop. The proposed research is aimed to achieve the reduced area; low power consumption and high stability for D flip flop which is used in phase locked loop (PLL). All this design D flip-flop is implemented by using 32nm CMOS technology.

A. Design of Conventional D Flip-Flop Using 32nm CMOS Technology:

D flip-flop is an important part of modern digital circuits. The conventional D flip-flop is design here by using 32nm CMOS technology in microwind 3.1 software. This design D flip-flop is used in phase locked loop. Circuit schematic of conventional D flip-flop is as shown in figure 4.1.

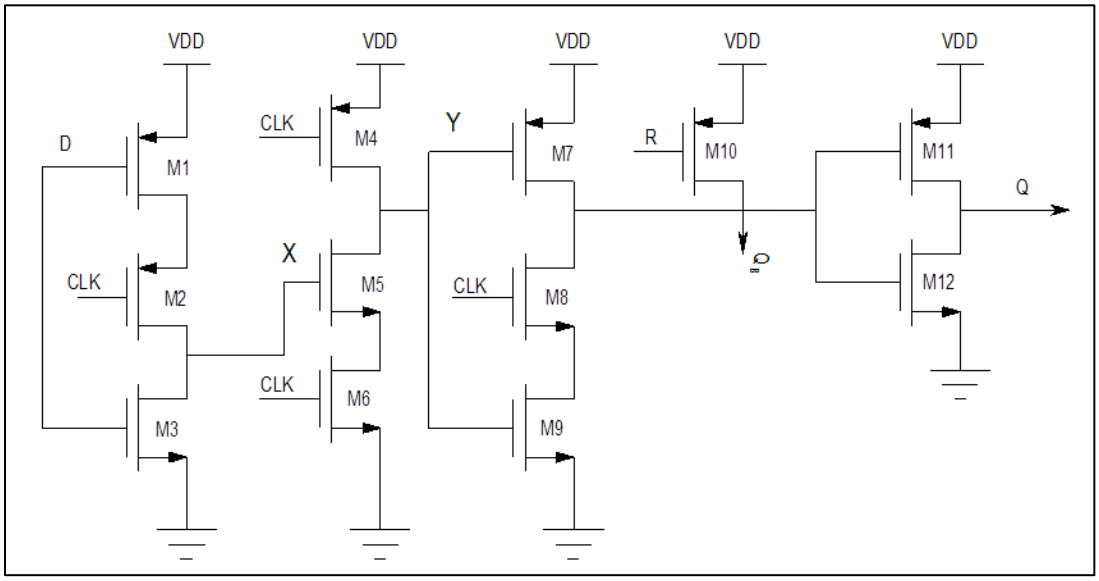

Fig. 4.1: Structure of conventional D flip-flop

Fig. 4.1 shows the design of a specialized single –phase edge triggered register. When clk=0, the input inverter is sampling the inverted D input on node X. The second (dynamic) inverter is in precharge mode, with M4 charging up node Y to VDD. The third inverter is in the hold mode, since M7 and M8 are off. Therefore during the low phase of the clock, the input of the final inverter holding its previous value and the output Q is stable. On the rising edge of the clk, the dynamic inverter M4-M6 evaluates. If X is high on the rising edge, node Y discharges. The third inverter M8-M9 is on during the high phase and the node value of Y is passed to the output Q. On the positive phase of clock, note that node X transitions to a low if the D input transition to a high level .Therefore the input must kept stable till the value on node X before the rising edge of the clock propagates to Y. This represents the hold time of register .transistor sizing is critical for achieving correct functionalities. The glitch problem can be corrected by resizing the pull down paths through M5-M6 and M8-M9.This design of dynamic flip flop also enable simple resetting M10 since the reset operation can performed by simple discharging one or two internal nodes.

Figure 4.2 shows the layout design of conventional D flip-flop using 32nm CMOS technology. This layout uses a power supply less than 1.20 volt dc. This layout is done using professional software Microwind. The layout has area 7.5µm2, which is small enough. Parasitic extraction and post simulation is performed successfully.

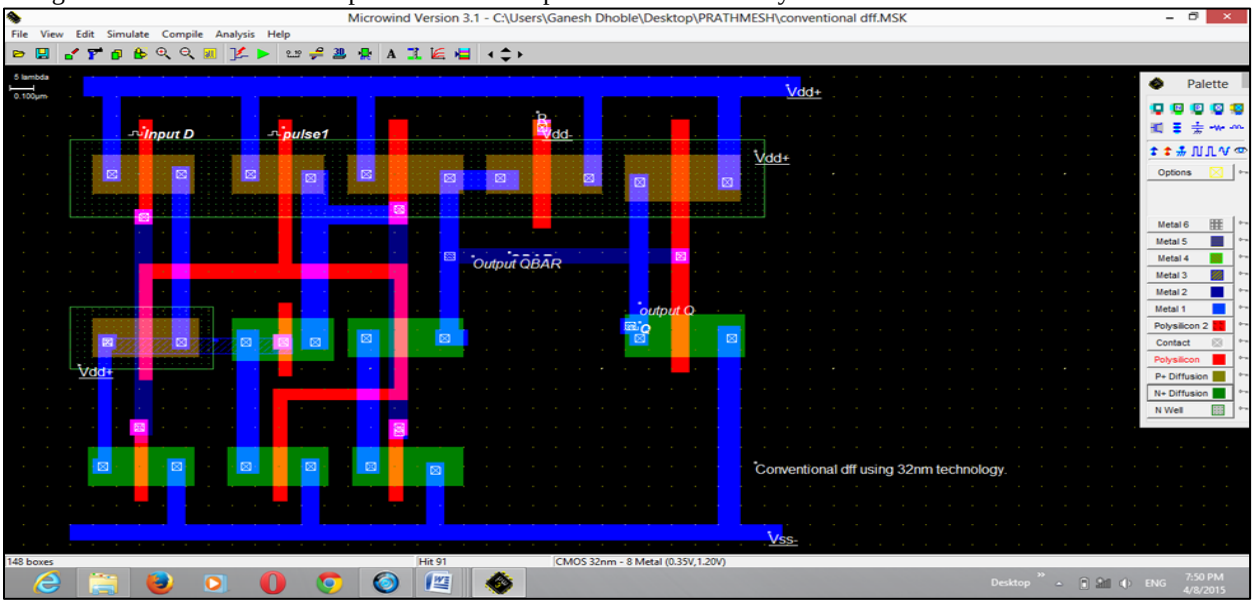

Fig 4.2: Layout of Conventional D flip-flop

The simulated output waveform of conventional D flip-flop for voltage vs. time is shown in Fig. 4.3. Simulations at the schematic level were performed using Microwind tool. Power consumption can be calculated from DC simulations. Simulated output voltage wave forms of differential time scale shown in figure 4.3.

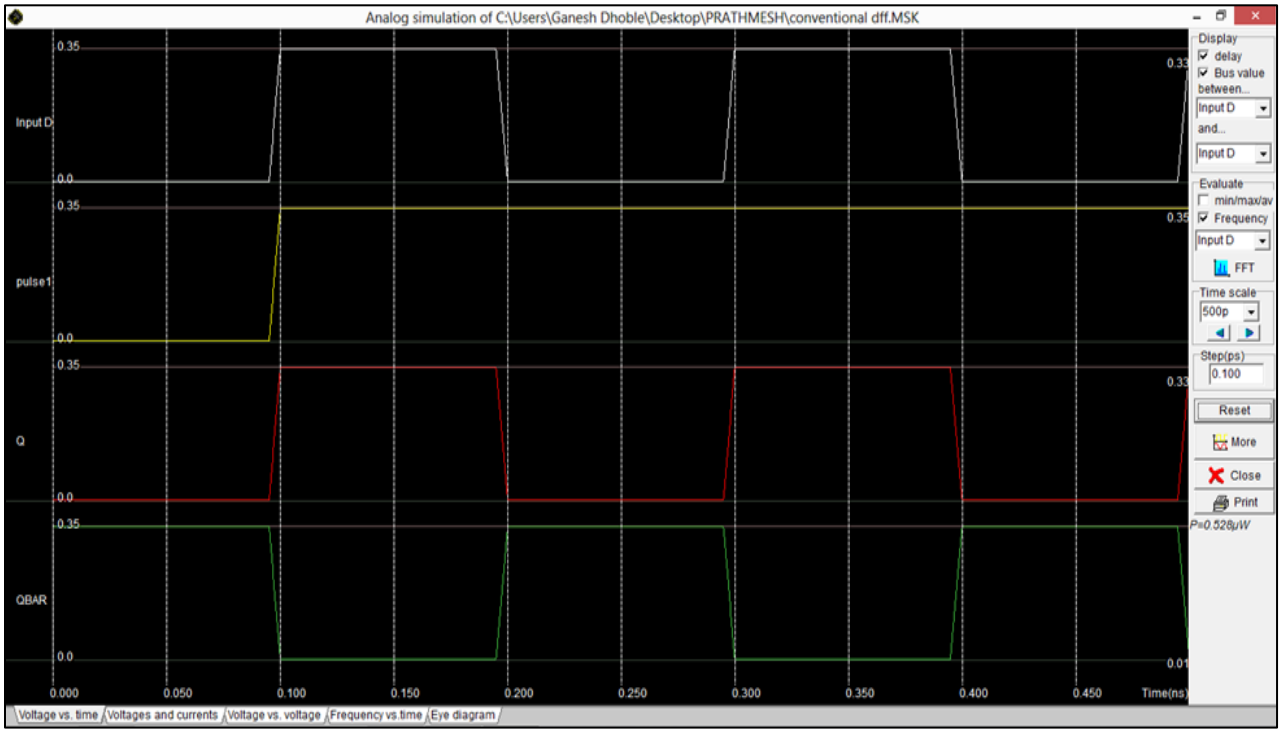

Fig. 4.3: Simulated output waveform of voltage verses time

Stimulated output waveform of conventional D flip-flop for voltage vs. current with differential output voltage as shown in Fig 4.4. Result obtain from simulation was Iddmax =0.007mA and current for N1 was 0.004mA. The Vdd supply is 0.3V min to 1.0V max. It is evidence that current depends on the input clock.

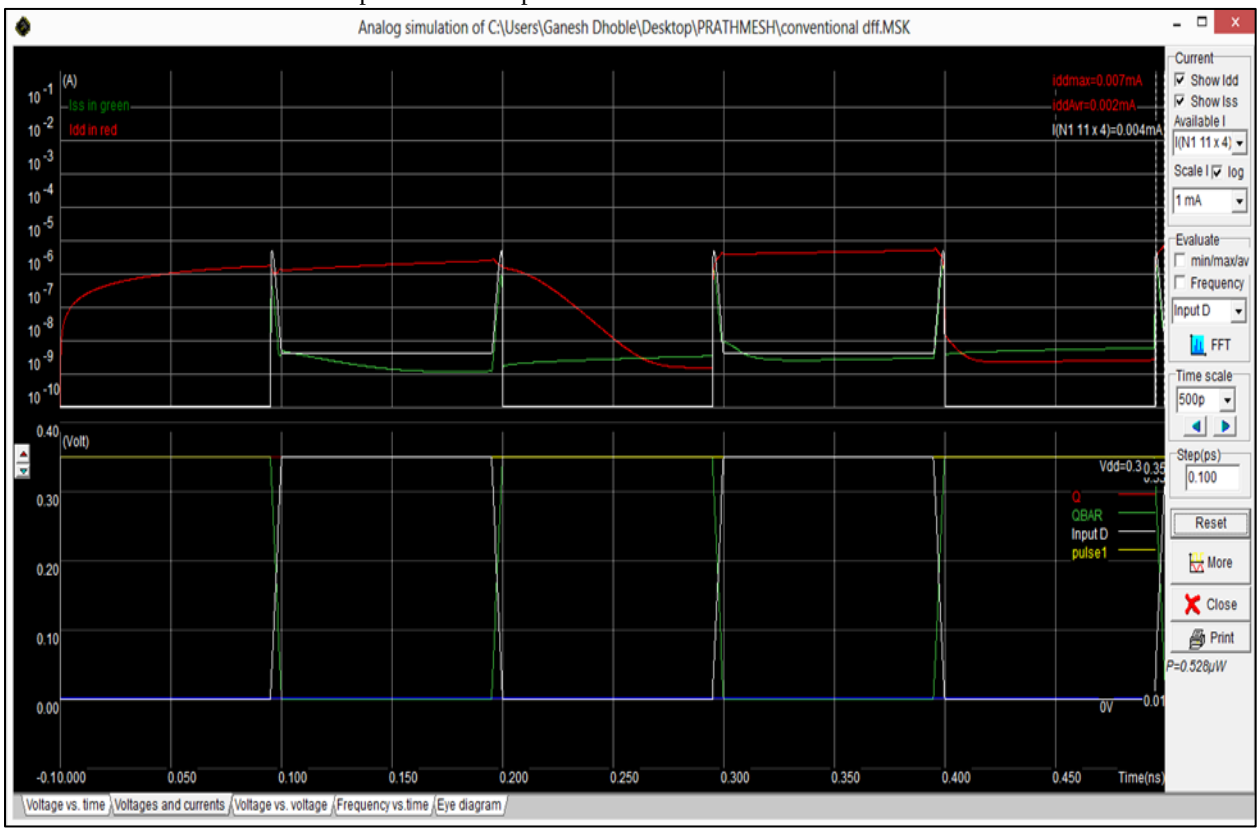

Fig. 4.4: Simulated output waveform of voltage verses current

Table 4.5 represented Observed output result for the different simulation of operational transresistance amplifier in Microwind 3.1 tool.

Table -4.5:
Output result obtain

Parameter Analysed	*Result obtain*
Input supply	*1.20*
Technology used	*32 nm CMOS technology*
Surface area	*7.5 um2*
Height	*2.4 um*
Width	*3.2 um*
No. of PMOS	*6*
No. of NMOS	*6*
Temperature	*27degree*
Power consumption	*0.528uW*

VI. CONCLUSION

In this way a high speed conventional D flip-flop is design. The D flip-flop was implemented in 32nm CMOS technology. The supply voltage was 1.2V. In this proposed circuit dynamic power consumption was reduced by lowering internal switching and speeds was increased by shortening input to output path. Also we used only 12 transistors to implemented conventional D flip-flop.

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