A novel high speed low power half adder cell is proposed in this paper. The critical path consist of an AND gate and an EX-OR gate. This cell offers higher speed, lower power consumption than the standard implementation of the half adder. In this paper a MTCMOS (Multi Threshold Complementary Metal Oxide Semiconductor) technique is proposed to reduce the leakage current and leakage power also and got better result as compared to standard half adder cell. MTCMOS is an effective circuit level technique that improves the performance and design low power cell by utilizing both low and high threshold voltage transistors. Leakage current of half adder is reduced by 50.24% using MTCMOS technique as compared to CMOS technique. Leakage power consumption of the half adder therefore reduced by 32.21% as compared to CMOS technique. All the simulation result based on 35 nm CMOS technology and simulated by cadence tool.

**Keywords:** Half Adder, High Speed, Low Power, MTCMOS, CMOS

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**I. INTRODUCTION**

The first monolithic integrated circuit (IC) was invented at Fairchild Semiconductor in 1959 [1], [2], [6]-[7]. The integration of an entire electrical circuit on a single piece of silicon significantly lowers the cost and enlarges the reliability as compared to the circuits with discrete components. The growth of the semiconductor industry driven by the advancements of the integrated circuit (IC) technology and the market dynamics was predicted by Gordon Moore in 1965 [1]-[3], [6]-[7]. A new process technology with significantly higher integration density and enhanced speed has been introduced by the semiconductor industry every two to three years since the early 1970s [1], [4], [6]-[7]. The size of the transistors is reduced with technology scaling, thereby increasing the integration density and the operating speed of the circuits [1], [5], [6]-[7].

A low power design is essential to achieve miniaturization and long battery life in battery-operated portable devices. With the current trend of semiconductor devices scaling into nanometre region, design challenges that were previously minor issues now become increasingly important where in the past dynamic power has been the major factor in CMOS digital circuit power consumption, recently with the dramatic decrease of supply and threshold voltages, a significant growth in leakage power demands new design methodologies for digital integrated circuits to meet the new power constraints. As one of the major components of leakage power, sub threshold leakage is caused by the current flowing the transistor even though it is turned off. The scaling down the feature size of the transistor exponentially increases the impact of sub threshold leakage.

Many techniques have been proposed to control or minimize leakage power in nanometre technology. Excessive power dissipation in integrated circuits, not only greatly affects their use in portable devices but also causes overheating, reduces chip life, functionality and degrades performance. Minimizing power consumption is therefore important and necessary, both for increasing levels of integration and to improve reliability, feasibility and cost [8]. Here we utilize MTCMOS technique for designing of high speed and power efficient half adder in 35 nanometre technology. MTCMOS technique has been emerged as a promising alternative to build logic circuits at a high speed with relatively small power dissipation as compared to traditional CMOS. MTCMOS is an effective circuit level technique that enhances the performance and provides low design methodologies by using both low and high threshold voltage transistors.

This paper is organized as follows section 2 gives a brief description of designing half adder using CMOS technique and section 3 presents proposed MTCMOS technique for half adder. Section 4 presents the details of leakage current and introduces leakage power of the half adder combinational circuit. Section 5 shows the simulation results of the half adder in terms of leakage current and leakage power & section 6 concludes this paper.

**II. IMPLEMENTATION OF HALF ADDER USING CMOS TECHNOLOGY**

Addition is the most basic arithmetic operation and adder is the most fundamental arithmetic component of the processor. The two important features of all digital circuits, for most applications are maximizing speed and minimizing power consumption. In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar.
Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two’s complement or ones complement is being used to represent negative numbers, it is trivial to modify an adder into an adder-subtractor. Other signed number representations require a more complex adder.

In digital circuit theory, combinational logic (sometimes also referred to as combinatorial logic) is a type of digital logic which is implemented by Boolean circuit, where the output is a pure function of the present input only. This is in contrast to sequential logic, in which the output depends not only on the present input but also on the history of the input. In other words, sequential logic has memory while combinational logic does not.

Combinational logic is used in computer circuits to do boolean algebra on input signals and on stored data. Practical computer circuits normally contain a mixture of combinational and sequential logic. For example, the part of an arithmetic logic unit, or ALU, that does mathematical calculations is constructed using combinational logic. Other circuits used in computers, such as half adders, full adders, half subtractors, full subtractors, multiplexer, demultiplexer, encoders and decoders are also made by using combinational logic.

A. Implementation of Half ADDER using Logic Gates:
The half adder is an example of a simple, functional digital circuit built from two logic gates. A half adder adds two one-bit binary numbers A and B. It has two outputs, Sum and Carry (the value theoretically carried on to the next addition). The simplest half-adder design, pictured in the fig, incorporates an XOR gate for Sum and an AND gate for Carry. Half adders cannot be used compositely, given their incapacity for a carry-in bit.

The simple addition consists of four possible elementary operations such as:

0+0=0
0+1=1
1+0=1
1+1=[1] 0 here 1 carry, 0 sum

The simplified Boolean functions for the outputs can be obtained directly from the truth table. The simplified sum of products expressions are

\[ \text{SUM} = A'B + AB' \]
\[ \text{CARRY} = AB \]
B. Logic gates description for Implementation of Half Adder:

1) XOR Gate:
The XOR gate (sometimes EOR gate, or EXOR gate) is a digital logic gate that implements an exclusive or; that is, a true output (1) results if one, and only one, of the inputs to the gate is true (1). If both inputs are false (0) and both are true (1), a false output (0) results. Its behavior is summarized in the truth table shown on the right. A way to remember XOR is "one or the other but not both". It represents the inequality function, i.e., the output is HIGH (1) if the inputs are not alike otherwise the output is LOW (0).

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
2) AND Gate:
The AND gate is a basic digital logic gates that implements logical conjunction- it behaves according to the truth table to the right. A HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH, a LOW output results. In another sense, the function of AND effectively finds the minimum between two binary digits, just as the OR function finds the maximum. Therefore, the output is always 0 except when all the inputs are 1s.
III. IMPLEMENTATION OF HALF ADDER USING MTCMOS TECHNIQUE

The scaling of CMOS technology in nanometer regime effectively reduces supply voltage and threshold voltage. Lowering of threshold voltages leads to an exponential increase in the sub threshold leakage current [9]. Excessive power dissipation in integrated circuits, not only greatly affects their use in portable devices but also causes overheating, reduces chip life, functionality and degrades performance. In the modern high performance integrated circuits, more than 40% of the active mode power is dissipated due to the leakage current. As number of the transistor increases on a chip, leakage current dominantly effects the total power consumption of the circuit.

The new MTCMOS circuit technology is proposed to satisfy both requirement of lowering the threshold voltage of transistor and reducing standby current, both which is necessary to obtain high speed and low power performance at the supply voltage. This technology has two main features. One is that NMOS& PMOS transistors with two different threshold voltages are employed in a single chip [10]. The other one is two operational mode active and sleep for efficient power management.

In MTCMOS technique, transistors of low threshold voltage become disconnected from power supply by using high threshold sleep transistor on the top and bottom of the logic circuit. Transistor having low threshold voltage (low-Vth) is used to design logic as shown in fig below. The sleep transistors are controlled by the sleep signal. During the active, the sleep signal is disserted, causing both high Vt transistor to turn on and provide a virtual power and ground to the low Vt logic. When the circuit is inactive sleep signal is asserted forcing both High Vt transistor to cut-off and disconnect power lines from the low Vt logic. This results a very low sub-threshold leakage current power to ground when the circuit is in standby mode. One drawback of this method is that portioning and sizing of sleep transistors is difficult for large circuits.

IV. LEAKAGE CURRENT AND LEAKAGE POWER

Leakage current/power is an important factor for any CMOS design circuit. The leakage current is directly related to the electric field of the device. By reducing the node voltages decrease the leakage current. In other words we can say that Leakage current/power is a waste charge of any device which is regularly discharging from the device even the device in off state. It reduces the capability of the device also became the reason of poor performance of device.
Leakage increases exponentially as the thickness of the insulating region decreases. Tunneling leakage can also occur across semiconductor junctions between heavily doped P-type and N-type semiconductors. Other than tunneling via the gate insulator or junctions, carriers can also leak between source and drain terminals of a Metal Oxide Semiconductor (MOS) transistor. This is called sub threshold conduction. The leakage current of a CMOS transistor consists of three main components: junction tunneling current, sub threshold current, and gate tunneling current. Leakage increases power consumption and if sufficiently large can cause complete circuit failure. Static CMOS gates are very power efficient because they dissipate nearly zero power when idle. Earlier, the power consumption of CMOS devices was not the major concern while designing chips. Factors like speed and area dominated the design parameters. As the CMOS technology moved below sub-micron levels the power consumption per unit area of the chip has risen tremendously. Here we use a CMOS technology to reduce the leakage current/power of half adder at 45 nanometer technology.

The leakage power is one of the major sources of power consumption in high performance cell. The leakage power dissipation is roughly proportional to the area of the circuit. The leakage power dissipation is expected to become a significant fraction of the overall chip power dissipation in nanometer CMOS design process [11]. In CMOS technology, standby power consists of leakage-power which increases with each silicon-technology generation [12]. Thus, for low-power devices, e.g. sensor nodes, standby leakage power reduction is crucial for device-operation within the scavenging power limit [13].

\[ P = \frac{1}{t} \int i \cdot v \, dt \]

This is the expression of power calculation. Where ‘P’ is the leakage power, ‘t’ is the time period, ‘i’ is the leakage current and ‘v’ is the supply voltage.

V. SIMULATION RESULTS

Half adder is a combinational circuit that performs the addition of two bits. In this paper we simulate half adder in 45 nanometer technology by cadence tool. Here we proposed MTCMOS technique that effectively reduces leakage current and leakage power of half adder circuit as compared to CMOS technique. From simulation results it is cleared that MTCMOS technique reduces leakage current by 56.55% and leakage power by 35.23.

![Image](image1.png)

![Image](image2.png)
<table>
<thead>
<tr>
<th>Half Adder</th>
<th>CMOS Technique</th>
<th>MTCMOS Technique</th>
<th>% Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage current(pA)</td>
<td>22.29</td>
<td>10.29</td>
<td>50.24</td>
</tr>
<tr>
<td>Leakage Power(nA)</td>
<td>1.722</td>
<td>1.22</td>
<td>32.21</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

In this paper we proposed a MTCMOS technique that greatly reduces the power dissipation of the half adder. Finally it is concluded that MTCMOS technique is better as compared to normal CMOS technique. MTCMOS is an effective circuit level technique that enhances the performance and provides low design methodologies by using both low and high threshold voltage transistors. From the simulation result it is cleared that after applying this technique we have reduced 56.55% in leakage current and 35.23% in leakage power.

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REFERENCES