Schematic Design and Process Variation of Low Power High Speed SRAM Cell and DRAM Cell using CMOS Sub-Micron Technology

Viplav A. Soliv
Assistant Professor
Department of Electronics and Telecommunication Engineering
Sipna College of Engineering and Technology, Amravati

Abstract

SRAM and DRAM cells have been the predominant technologies used to implement memory cells in computer systems. This paper deals with the design and analysis of high speed Static Random Access Memory (SRAM) Cell and Dynamic Random Access Memory (DRAM) Cell to perform high speed to develop low power consumption. SRAM cells are faster and require no refresh since reads are not destructive. In contrast, DRAM cells provide higher density and minimal leakage energy. Here we use 6-transistor SRAM cell built from a simple static latch and tri state inverter and 3-transistor DRAM cell. The reading action itself refreshes the content of memory. The SRAM access path is split into two portions: from address input to word line rise (the row decoder) and from word line rise to data output (the read data path). The decoder which constitutes the path from address input to the word line rise is implemented as a binary structure by implementing a multi-stage path. The key to low power operation in the SRAM data path is to reduce the signal swings on the high capacitance nodes like the bit lines and the data lines. Results show good performance.

Keywords: 6T SRAM cell, Low power, SRAM, 3T1D DRAM

I. INTRODUCTION

A. General Introduction:

Memory circuits are generally classified according to the type of data storage and the type of the data access. Read/Write Memory circuit must permit the modification (writing) of data bits stored in the memory array, as well as their retrieval (reading) on demand. This requires that the data storage function be volatile. i.e. the stored data are lost when the power supply voltage is turned off. The read-write memory circuits are called as Random Access Memory (RAM). Compared to sequential-access memories such as magnetic tapes, any cell in the R/W memory array can be accessed with nearly equal access time. [7]

A typical memory array organization is shown in figure 1. The data storage structure, or core, consists of individual memory cells arranged in an array of horizontal rows and vertical columns. Each cell is capable of storing one bit of binary information. Also, each memory cell shares a common connection with the other cells in the same row, and another common connection with the other cells in the same column. In this structure, there are 2 rows, also called word lines, and 2M columns, also called bit lines. Thus, the total number of memory cells in this array is 2 x 2. [6]

To access a particular memory cell, i.e., a particular data bit in this array, the corresponding bit line and the corresponding word line must be activated (selected). The row decoder circuit selects one out of 2N word lines according to an N bit row address, while the column decoder circuit selects one out of 2M bit lines according to an M-bit column address. Once a memory cell or a group of memory cells are selected in this fashion, a data read and/or a data write operation may be performed on the selected single bit or multiple bits on a particular row. The column decoder circuit serves the double duties of selecting the particular columns and routing the corresponding data content in a selected row to the output. [8]

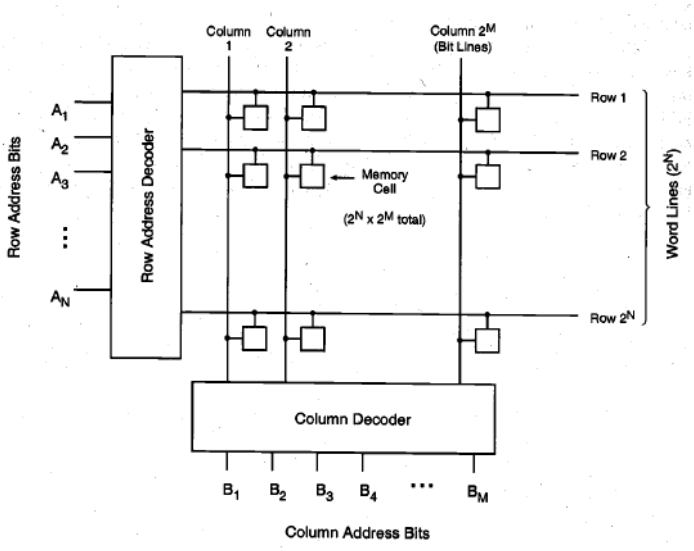

Fig. 1: Typical Random Access Memory Array Organization

The memory circuit is said to be static if the stored data can be retained indefinitely, without any need for a periodic refresh operation. The data storage cell, i.e., the 1-bit memory cell in static RAM arrays, it consists of a simple latch circuit with two stable operating points (states). Cache memories occupy an important percentage of the overall die area.

B. CMOS Sub-Micron Technology:

CMOS submicron technologies are today widely used in mixed-signal front-end systems. From the discrete semiconductor component technology, the transition from the past focused on a major reduction in device size. This trend has given rise to the acronyms SSI, MSI, LSI, and VLSI standing for small scale, medium scale, large scale, and very large scale integration, respectively. We consider four main generations of integrated circuit technologies: micron, submicron, deep submicron and ultra deep submicron technologies. [6]

The deep submicron technology started with the introduction of lithography better than 0.3µm. ultra deep submicron technology concerns lithography below 0.1µm. Four topics impacting our ability to achieve these levels, These are shrinking of conductor and device dimensions, known as scaling, reliability concerns in small structures, representative processes utilized in achieving small structures, and anticipated circuit delays for Insulated-Gate Field-Effect Transistors, IGFET's, at 1-µm design ground rules. The most interesting topologies are analyzed and compared for speed, power consumption, and power-delay product. The comparison has been performed on two classes of circuits, the former with minimum transistor size to minimize power consumption, the latter with optimized transistor dimension to minimize power-delay product. Performance has been also compared for different supply voltage values. The characterization has been extended to CMOS processes with minimum channel length of 350, 250, 180, 130, 90 and 65 nm technologies. Noise measurements, both in the drain and in the gate current, are carried out by means of purposely developed wide band trans impedance amplifiers. Special attention is given to the behavior of white and 1/f components in the noise voltage spectrum. [6]

C. An Introduction to SRAM:

The fundamental building block of a static RAM is the SRAM memory cell. The cell is activated by raising the word line and is read or written through the bit line. SRAM is designed to fill two needs: to provide a direct interface with the CPU systems that require very low power consumption. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU. A read-write (R/W) memory circuits are designed to permit the modification (writing) of data bits to be stored in the memory array, as well as their retrieval (reading) on demand. The memory circuit is said to be static if the stored data can be retained indefinitely, without any need for a periodic refresh operation. We have examined the circuit structure and the operation of simple SRAM cells.

D. An Introduction to DRAM:

Dynamic random-access memory (DRAM) is a type of random-access memory that stores each bit of data in a separate capacitor within an integrated circuit. The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, conventionally called 0 and 1. Since capacitors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory. The main memory ("RAM") in personal computers is DRAM. It is the RAM in laptop and workstation computers as well as some of the RAM of video game consoles. Unlike flash memory, DRAM is volatile memory, since it loses its data quickly when power is removed. The transistors and capacitors used are extremely small; billions can fit on a single memory chip.

II. SCHEMATIC MEMORY DESIGN ARCHITECTURE

A. Schematic Memory Design Architecture:

The preferred architecture for Random access memories is shown in Figure 2. The name is derived from the fact that memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing. The storage array, or core, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical columns. The horizontal lines, which are driven only from outside the storage array, are called word lines, while the vertical lines, along which data flow into and out of cells, are called bit lines.

A cell is accessed for reading or writing by selecting its row and column. Each Cell can store 0 or 1. Memories may simultaneously select 4, 8, 16, 32, or 64columns in one row depending on the application. The row and column to be selected are determined by decoding binary address information. In this design, the number of rows and columns, both are equal to 64 for 4Mb memory cut. Using two such memory cuts, a 8Mb SRAM memory is designed. It consists of Inverter, Decoder Circuit, Decoder driver circuit, Wrlogic circuit, SRAM Cell and the sense amplifier. Here the ami 0.60µm technology is used with supply voltage is of 3V. The two inverters (A0, A0B, A1, A1B) are use to change the binary logical values (0,1) and the output of this inverter is get connected to Decoder (2:4 Decoder). The number of SRAM Cell is depending upon decoder (4 SRAM Cell, 2:4 Decoder). SRAM Cell is heart of SRAM memory circuit. Here the sense amplifier is used to sense the logical data using b and bb.

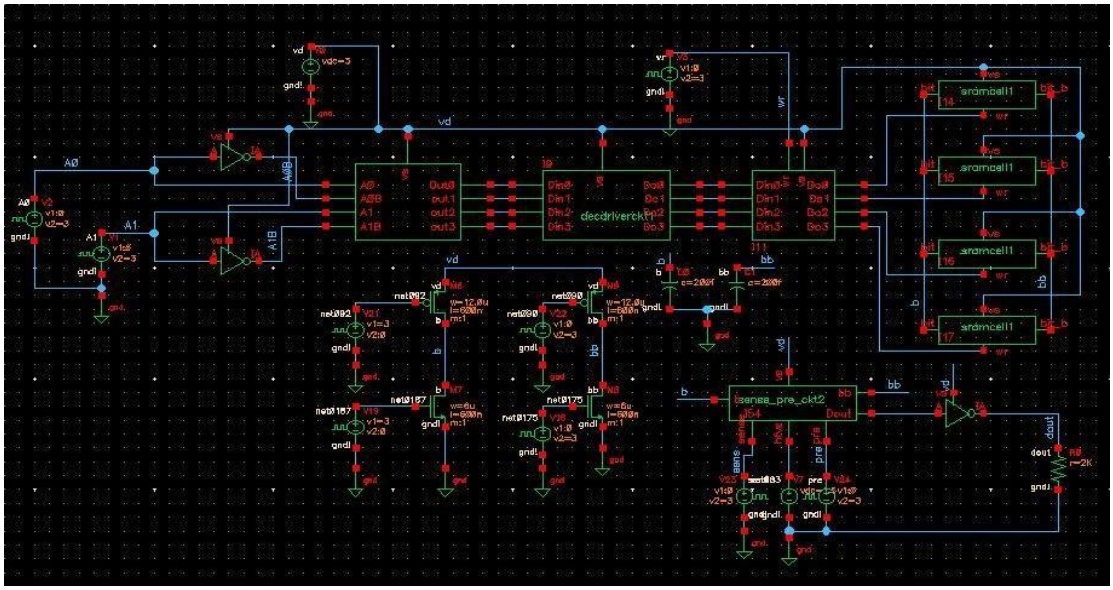

Fig. 2: SRAM Memory Design Architecture

1) *SRAM Cell Architecture (6T):*

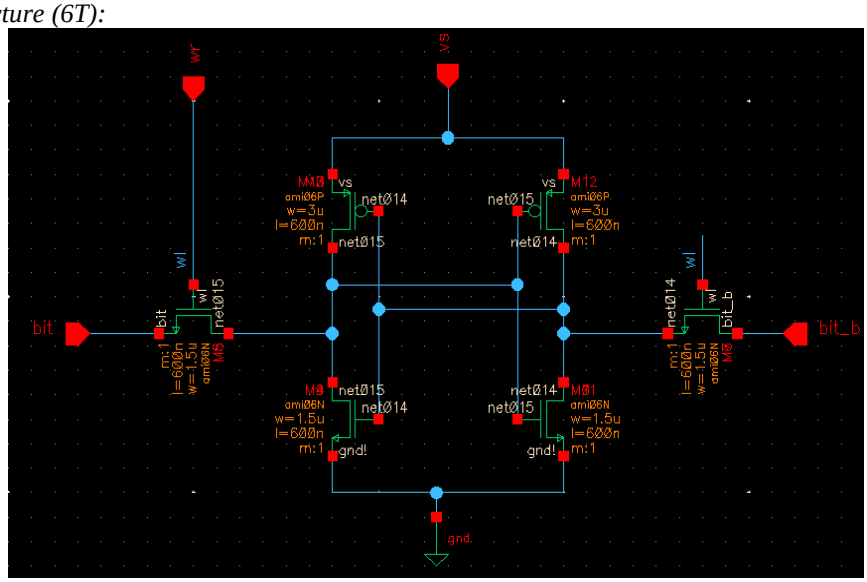

Fig. 3: 6T-SRAM Cell Architecture

The Figure 3 shows 6T-SRAM cell architecture. Six-transistor (6T)-based SRAM continues to play a pivotal role in nearly all VLSI systems due to its superior speed and full compatibility with logic process technology. When the cell is not addressed, the two access transistors are closed and the data is kept to a stable state, latched within the flip-flop. The flip-flop needs the power supply to keep the information. The SRAM cell consists of a bi-stable flip-flop connected to the internal circuitry by two access transistors. A low-power SRAM cell may be designed simply by using cross-coupled. Other advantages of CMOS SRAM cells include high noise immunity due to larger noise margins, and the ability to operate at lower power supply voltages. [7]

2) *SRAM Cell Read/Write operation:*

Figure 4 shows the read/write operations of an SRAM cell. To select a cell, the two access transistors must be "on" so the elementary cell can be connected to the internal SRAM circuitry. These two access transistors of a cell are connected to the word line. The selected row will be set at VCC. The two flip-flop sides are thus connected to a pair of lines, B and B. The bit lines are also called columns or Y addresses. During a read operation these two bit lines are connected to the sense amplifier that recognizes if a logic data "1" or "0" is stored in the selected elementary cell. This sense amplifier then transfers the logic state to the output buffer which is connected to the output pad. There are as many sense amplifiers as there are output pads. Read cycle starts with pre-charging BL and BLB to 1, i.e., VDD. Within the memory cell M1 and M4 are ON. Asserting the word line, turns ON the M5 and M6 and the values of Q and Q are transferred to Bit-Lines. No current flows through M6, thus M4 and M6 pull BL up to VDD, i.e., BL = 1 and BLB discharges through M1 and M5. This voltage difference is sensed and amplified to logic levels by sense amplifiers. [6]

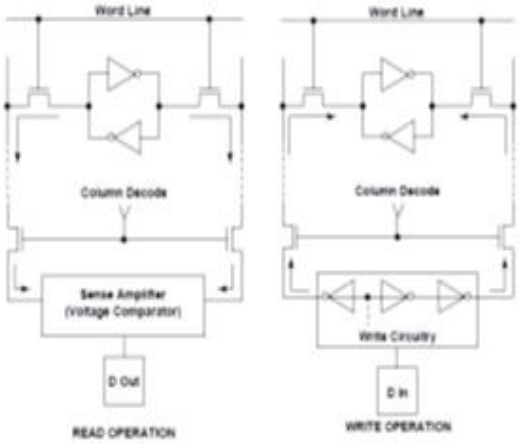

Fig. 4: SRAM Cell Read/Write Operation

During a write operation, data comes from the input pad. It then moves to the write circuitry. Since the write circuitry drivers are stronger than the cell flip-flop transistors, the data will be forced onto the cell. When the read/write operation is completed, the word line is set to 0V, the cell either keeps its original data for a read cycle or stores the new data which was loaded during the write cycle. The value to be written is applied to the Bit lines. Thus to write data '0', we assert BL='0', BLB = '1' and to write data '1', the BL = '1', BLB = '0', asserted when WL = 1. [7]

B. DRAM Memory Design Architecture:

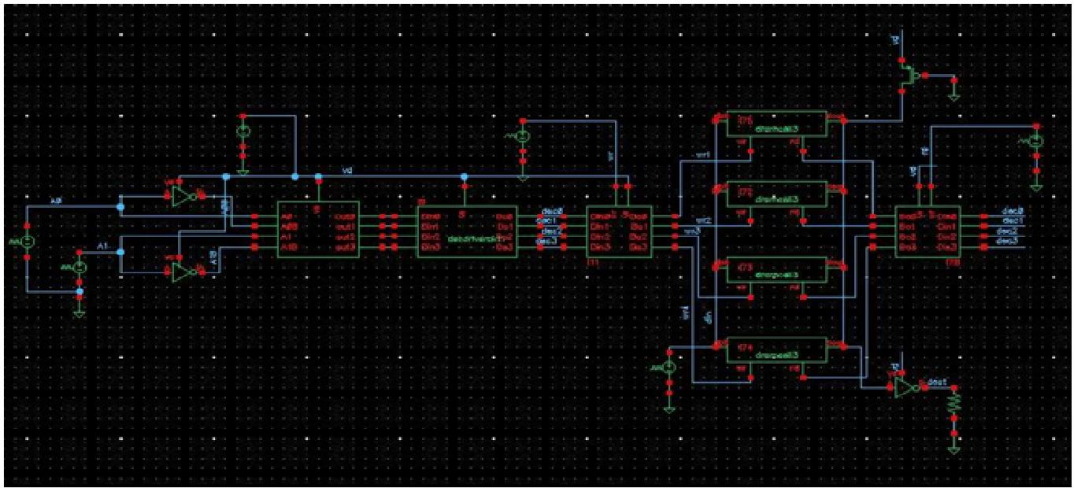

Fig. 5: DRAM Memory Design Architecture

Figure 5 shows DRAM memory design architecture consist of DRAM cell, Decoder circuit, Decoder driver ckt, sense amplifier, wrlogic ckt. The basis of the storage system is the charge placed in node S, written from BLwrite line when T1 is

activated. Consequently, it has a DRAM cell nature, but it allows a non-destructive read process and a high performance read and writes operation. With T1 and T3 transistors as accessing devices, the whole cell is composed by four transistors. This implies a more compact cell structure. In order to write the cell at the BLwrite line level, it is only required to activate T1 through the WLwrite line. Hence, the S node stores either a 0 or a Vdd−Vth voltage, Depending on the logic value. This voltage results in the accumulation of charge at the gate of devices D1 and T2.

1) *DRAM Cell Architecture (3T):*

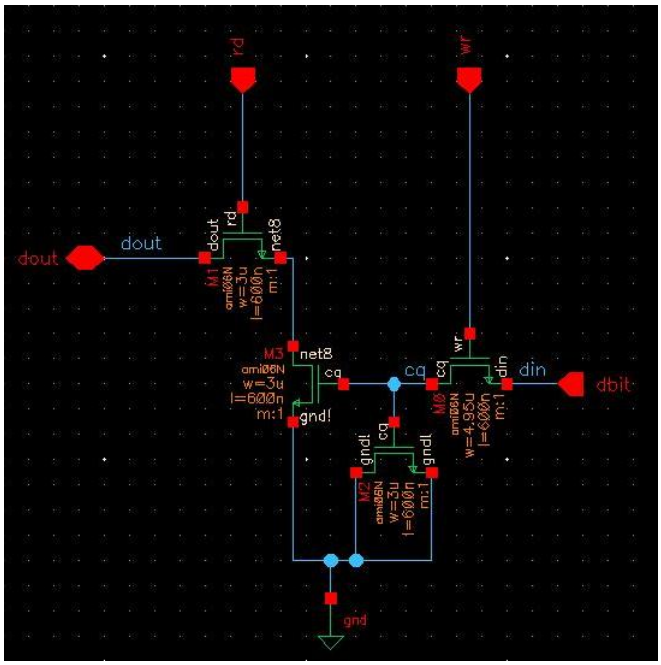

Fig. 6: DRAM 3T1D-Cell Architecture

The 3T1D cell Figure 6 shows the scheme of the basic cell. A key aspect of the 3T1D memory cell is that the capacitance of the gated diode (D1) when Vgs is above Vth is significantly higher with respect to lower voltages, because there is a substantial amount of charge stored in the inversion layer. If the node S is storing a high logic value (Vdd−Vth) when the voltage at the source of the gated diode is raised there is a large voltage increase in the node S and the transistor T2 is switched on. In order to read the cell, the read bitline BLread has to be previously precharged at Vdd level. Then T3 is activated from WLread line. If a high (1) level is stored in S, transistor T2 turns on and discharges the bitline. If a low (0) level is stored in S, transistor T2 does not reach enough conduction level. The objective of the gated diode D1 is to improve Read Access Time. When a high (1) level is stored in S, D1 connected to WLread line causes a boosting effect of the voltage level in node S. The voltage level reached at node S is close to Vdd voltage causing a fast discharge of the parasitic capacitance in BLread. [3]

2) *DRAM Cell Read/Write Operation:*

The sense amplifiers are disconnected to the bit-lines. The bit-lines are recharged to exactly equal voltages that are in between high and low logic levels. The bit-lines are physically symmetrical to keep the capacitance equal, and therefore the voltages are equal. The desired row's word-line is then driven high to connect a cell's storage capacitor to its bit-line. If the storage cell's capacitor is discharged, it will greatly decrease the voltage on the bit-line as the pre-charge is used to charge the storage capacitor. If the storage cell is charged, the bit-line's voltage only decreases very slightly.

The sense amplifiers are connected to the bit-lines. Positive feedback then occurs from the cross-connected inverters, thereby amplifying the small voltage difference between the odd and even row bit-lines of a particular column until one bit line is fully at the lowest voltage and the other is at the maximum high voltage. Once this has happened, the row is "open". All storage cells in the open row are sensed simultaneously, and the sense amplifier outputs latched. A column address then selects which latch bit to connect to the external data bus. Reads of different columns in the same row can be performed without a row opening delay because, for the open row, all data has already been sensed and latched. While reading of columns in a open row is occurring, current is flowing back up the bit-lines from the output of the sense amplifiers and recharging the storage cells. This refreshes the charge in the storage cell by increasing the voltage in the storage capacitor if it was charged to begin with, or by keeping it discharged if it was empty. When done with reading all the columns in the current open row, the word-line is switched off to disconnect the storage cell capacitors; the row is "closed" from the bit-lines. The sense amplifier is switched off, and the bit lines are pre-charged again.

To store data, a row is opened and a given column's sense amplifier is temporarily forced to the desired high or low voltage state, thus causing the bit-line to charge or discharge the cell storage capacitor to the desired value. Due to sense amplifier's positive feedback configuration, it will hold a bit-line at stable voltage even after the forcing voltage is removed. During a write

to a particular cell, all the columns in a row are sensed simultaneously just as during reading, so although only a single column's storage-cell capacitor charge is changed, the entire row is refreshed.

III. PROCESS VARIATION

A. Technology Variation:

The main purpose of Technology variation is to determine the efficiency of 6T SRAM Cells & 3T1D DRAM Cells by varying the technology of ami & tsmc. The technology varies are:-

1) AMI 0.6um (American Microsystems Incorporation)
2) TSMC 0.4um & o.3um (Taiwan Semiconductor Manufacturing Company)
3) 0.6 um SRAM 4x1 Memory cell

This is a methodology and service combination, design for manufacturability starting from gate level, all the way to final routed GDS. A nanometer design solution accelerates first time silicon success. Cadences have been providing a total nanometer design solution. Cadence is a full-line distributor of the TSMC 30, 40/45, 65, 90, 130, 150-nanometer and Nexsys 90-nanometer standard cell libraries and standard I/O libraries.

B. Voltage Variation:

Voltage variation can be obtained by changing the Scale/ Voltage of all Schematics of ami & tsmc technology and Observed the Outputs. It has been observed that by changing the voltage scale 3.5 V, 3V & 2.5 V, Outputs of 4x1 Memory Cells are efficient and Respective Power Consumption is also calculated.

IV. SIMULATION ENVIRONMENT AND RESULTS

A. Simulation of 6T SRAM 4x1 Memory Cell:

1) *Results of 6T SRAM for 0.60um ami:*

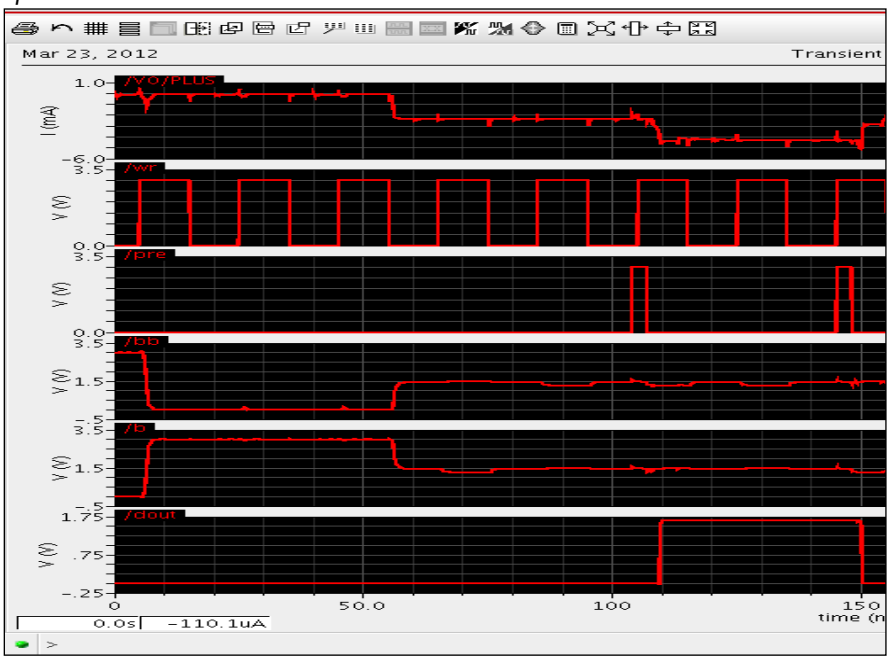

Fig. 7: Results of 6T SRAM For 0.6 um ami

B. Simulation of 3T1D Dram Cell:

1) *Results of 3T1D DRAM For 0.60um ami:*

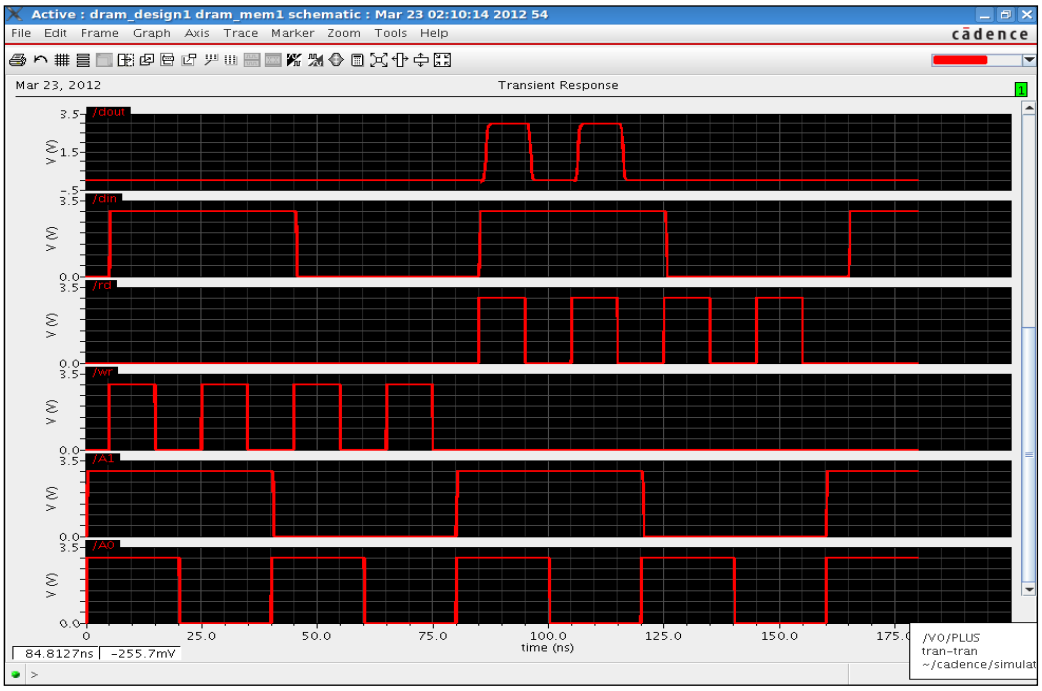

Fig. 8: Results of 3T1D DRAM for 0.60um ami

C. Scale Variation & Power Calculation for SRAM:

The following table shows that as variations in technology like (0.60u ami, 0.40u tsmc, 0.30u tsmc) the current in (mA, uA) and power in (mW, uW) will be varied in SRAM Cell and DRAM Cell.

1) *Voltage Variation at 3.5V:*

Table – 1
Voltage Variation At 3.5V

Technology	*SRAM*		*DRAM*	
	Current	*Power*	*Current*	*Power*
0.60u ami	*5.9mA*	*20.65mW*	*375uA*	*1313uW*
0.40u tsmc	*4 mA*	*14mW*	*355uA*	*1243uW*
0.30u tsmc	*8mA*	*28mW*	*484uA*	*1694uW*

2) *Voltage Variation at 3V:*

Table – 2
Voltage Variation at 3V

Technology	*SRAM*		*DRAM*	
	Current	*Power*	*Current*	*Power*
0.60u ami	*108uA*	*324uW*	*107uA*	*321uW*
0.40u tsmc	*120uA*	*360uW*	*124uA*	*372uW*
0.30u tsmc	*165uA*	*495uW*	*165uA*	*495uw*

3) *Voltage Variation at 2.5 V:*

Table – 3
Voltage Variation at 2.5V

Technology	*SRAM*		*DRAM*	
	Current	*Power*	*Current*	*Power*
0.60u ami	*1.5mA*	*3.75mW*	*46uA*	*115uW*
0.40u tsmc	*2.4mA*	*6mW*	*180uA*	*450uW*
0.30u tsmc	*4.5mA*	*11.25 mW*	*115uA*	*287uw*

V. CONCLUSION

The work in this paper is dedicated to the investigation of memory system performance characteristics, and the result of the investigation is then used to evaluate and support the design of future Memory devices. The result of the imbalance in performance scaling trends between processor and memory is that modern computer systems are increasingly constrained by the performance of memory systems. This dissertation presents the design and analysis of 6T SRAM Cells & 3T1D DRAM Cells have very low power consumption. Transient and parametric analyses were carried out in the simulation process.

From the above results of Power calculation of SRAM Cell & 3TID DRAM Cell of the different technologies, it is observed that power consumption increases as length and width of the transistor decreases. It is because when the aspect ratio of MOS decreases the gate loses control over the current, hence the overall power consumption increases. In order to reduce the power consumption we have to use more than one gated MOS concept known as FIN to control the current over gate.

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