An Optimal Design of Ring Oscillator and Differential LC using 45 nm CMOS Technology

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Abstract

Robust, high performance oscillator design in CMOS technology continues to pose interesting challenges. CMOS circuitry in VLSI dissipates less power during static, and is denser than any other implementations having the similar functionality.This paper provides a new approach for the physical design of ring and differential LC oscillator are designed with CMOS 45 nm technology with Microwind 3.5 EDA tool. The circuits are easy to be integrated and with low power consumption. The presented results are obtained using CMOS EDA tool Microwind 3.5. Also the calculated results are obtained with the working formulas for the structures. In this paper, we compare the on screen simulated and calculated results.

Keywords: CMOS 45 nm, Ring Oscillator, LC oscillator, on screen and calculated frequencies

I. INTRODUCTION

As the area of electronic devices is shrinking with time and VLSI technology shift towards nanometer feature sizes which interconnect in the order of delays and leakage power, dominating gate delays and dominating power. High performance and low power circuit design face many challenges. One of the key issue is high-speed storage media design is accomplishing very low cycle times and reducing leakage power consumption. We have dealt with the design approaches and circuit techniques and provided a detailed failure analysis to improve the reliability of low power and high speed SRAMs. The motive behind this is to provide a cost-effective and better way to develop ultra-low power memory system.

An oscillator is an electronic device used for the purpose of generation of a signal with specific frequency. Robust, high performance oscillator design in CMOS technology continues to pose interesting challenges. CMOS circuitry in VLSI dissipates less power during static, and is denser than any other implementations having the similar functionality.

An oscillator circuit produces a periodic signal without any input signal. It converts DC power, from the supply, to a periodic signal. Oscillators are extensively used in both receive and transmit paths. They are used to provide the local oscillation for the mixers for up and down conversion. Oscillators are a fundamental part in many electronic systems. Applications utilize oscillators range from clock generation in microprocessors to frequency translation in mobile phones. Different application also requires different set of oscillator performance parameters.

With the fast advancement of CMOS technology, more & more signal processing functions are implemented in the digital domain for low cost, low power consumption, higher yield, & higher re-configurability.

There are many CMOS based oscillators available in the market. Here we have decided to study and physical design analysis the two different oscillators as;

1) Ring Oscillator:
2) Differential LC oscillator

As per prior designing concept, the ring oscillator consists of odd number of inverter stages. The output frequency is equal to the inverse of the propagation delay of all the inverters. The output of the last inverter is fed as the input to the first inverter.

A LC circuit is a resonant circuit, tank circuit or tuned circuit consisting of L and C connected together. It is used for the generation of signals at a particular frequency. Frequency is controlled using L and C components. Differential LC circuit has many advantages, such as simple structure, high operating frequency and good linearity relationship between L and C values and frequency of oscillation.

II. DESIGN OF RING OSCILLATOR

The role of ring oscillators is to create a periodic logic or analog signal with a stable and predictable frequency. The ring oscillator is a very simple oscillator circuit, based on the switching delay existing between the input and output of an inverter. If an odd chain of inverters are connected, a natural oscillation is obtained, with a period which corresponds roughly to the number of elementary delays per gate. The fastest oscillation is obtained with 3 inverters. One single inverter connected to itself does not oscillate. The usual implementation consists in a series of five up to one hundred chained inverters.

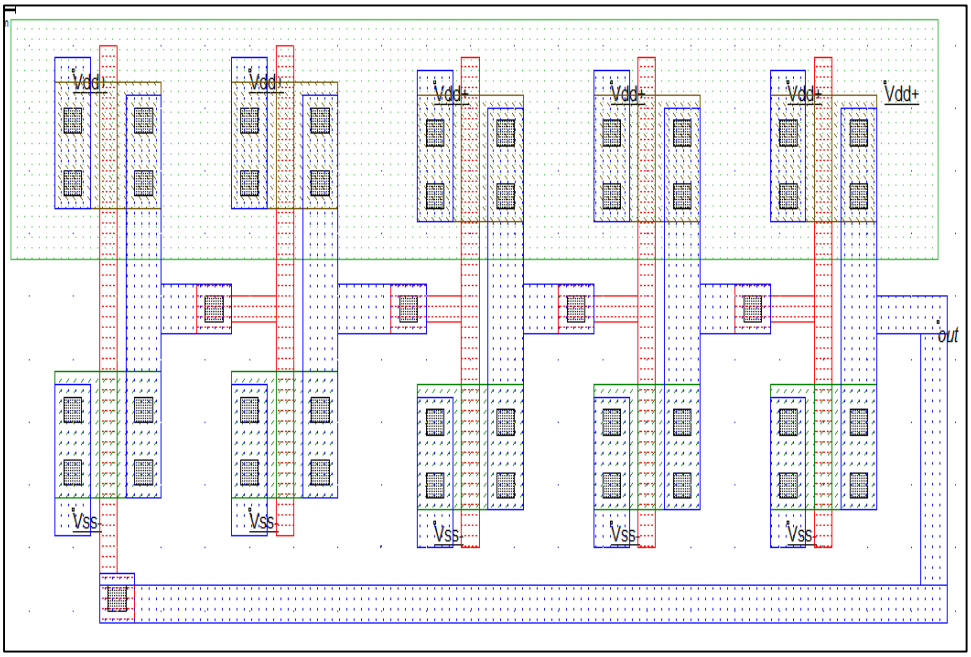

Fig. 1: Physical design of Ring Oscillator

The ring oscillator made from five inverters has the property of oscillating naturally. The output oscillating frequency is equal to the inverse of the propagation delay of all inverters. It is a device composed of an odd number of inverters attached in a chain, with the output of the last inverter fed back into the first. The output oscillates between two voltage levels, representing true and false. The oscillations are due to the switching delay existing between the input and the output of each inverter. The fastest oscillation is obtained with the minimum number of inverters which is 3, because it doesn't oscillate with only one.

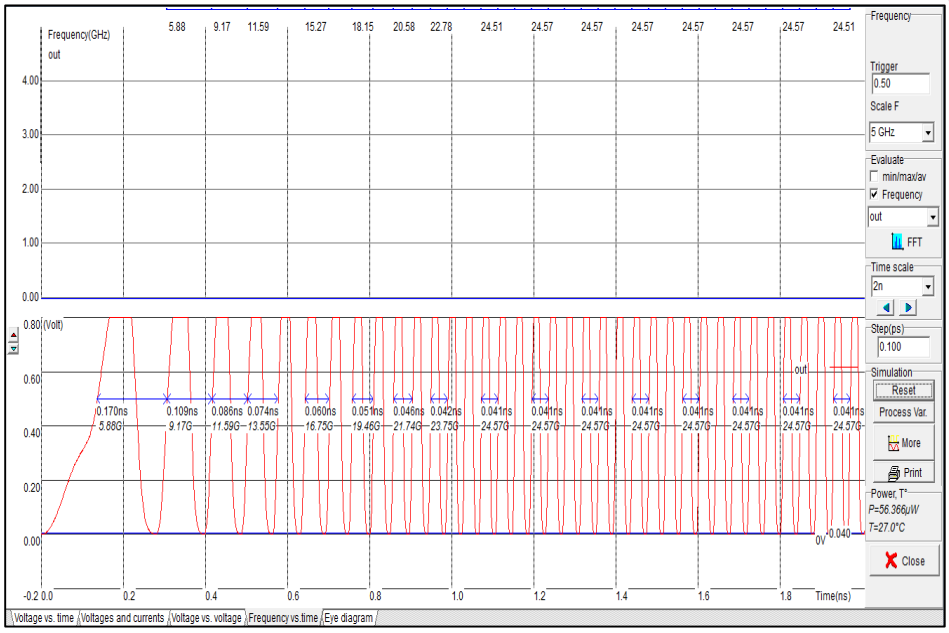

Fig. 2: Frequency vs Time curve

From the simulation shown in figure 2, the oscillating frequency is 24.57 GHz.

A. Calculated Frequency for Ring Oscillator:

For calculating the oscillating frequency according the number of stages of inverter;

For 45 nm Technology, by default minimum width and length are as

For PMOS

- Width (W) = 0.200 um
- Length (L) = 0.040 um
- For these values of W & L, the current Imax is 0.086 mA

Same, For 45 nm Technology, by default minimum width and length are as,

For NMOS

- Width (W) = 0.200 um
- Length (L) = 0.040 um
- For these values of W & L, the current Imax is 0.147 mA

By implementing these values and by generating the PMOS and NMOS transistor with the help of Microwind EDA tool software, we are coming across the simulation result for single stage.

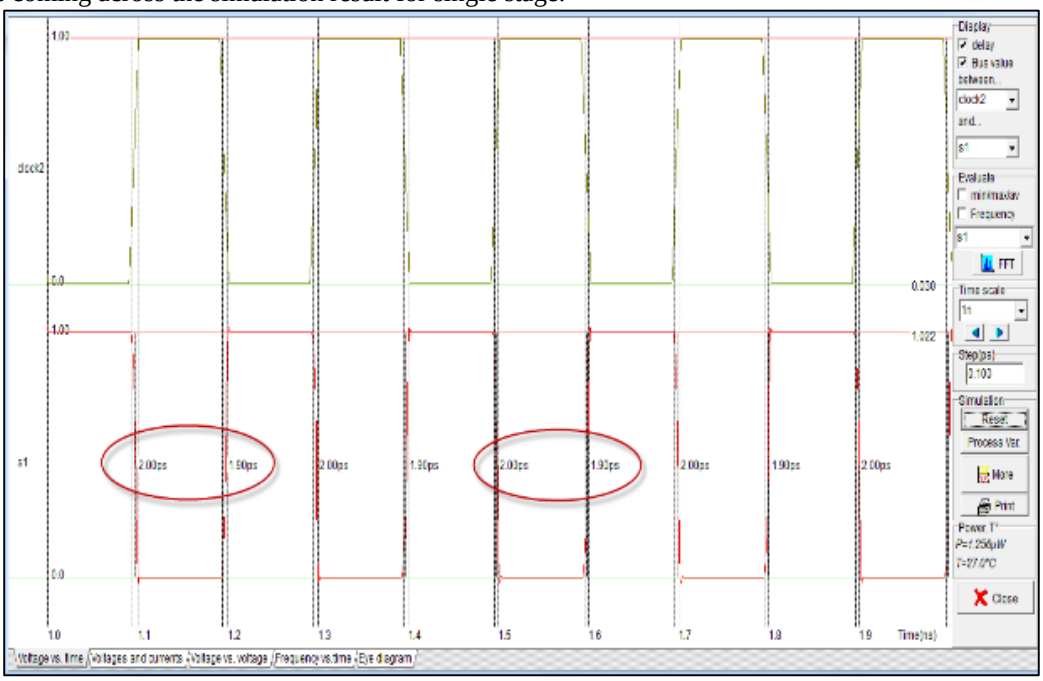

Fig. 3: Propagation delay finding for single stage

For finding out the propagation delay for one cycle, we need the rise time and fall time.

Here, from the figure, in our design simulation, the Tr is 2 nsec and Tf is 1.9 nsec. For on paper calculation of oscillating frequency for 5 stages,

$$fosc = \frac{1}{2Nstages(tD)}$$

Where:

fo= frequency of oscillations

N" = number of stages

tD =propagation/ Switching Delays

B. Calculated Frequency

$$fosc = \frac{1}{2Nstages((tDhl+tDlh))}$$

Where;

fo= frequency of oscillations

N = number of stages

τdhl= output propagation for high to low delay time.

τdhl=output propagation for low to high delay time.

Putting the Values in the equestion;

$$fosc = \frac{1}{2Nstages((tDhl+tDlh))}$$

$$\frac{1}{10 * (3.9 * 10\text{^} - 12)}$$

= 24.64 GHz.

Also practical implementations of Multi valued logic arithmetic will provides advantages which are very wide and very feasible for number representation, processors designing, communication network, electronics converters and Memory designing.

Calculated Oscillating frequency for 5 stages ring oscillator (RO) for 45nm technology, we are getting as 25.64 GHz. Similarly we can put down the values for odd number of stages and you can find out the oscillation frequency.

For Ring oscillator with odd number of stages as 9, 11, and 13, we are coming across calculated oscillating frequency as 14.24 GHz, 11.65 GHz, and 9.86 GHz respectively.

III. DIFFERENTIAL LC OSCILLATOR:

LC oscillators are commonly used in radio frequency circuits because of their good phase noise characteristics and their ease of implementation. An oscillator has a small signal feedback amplifier, with an open loop gain equal to or slightly greater than one for oscillations to start. But to continue oscillations, the average loop gain must return to unity. In addition to these reactive components, an amplifying device such as an Operational Amplifier or Bipolar Transistor is required. Unlike an amplifier, there is no external AC input required to cause the Oscillator to work as the DC supply energy is converted by the oscillator into AC energy at the required frequency. Differential LC oscillator the operating frequency is decided by the capacitor and inductor value.

The operating frequency is given by:

$$fo = \frac{\omega 0}{2\pi} = \frac{1}{2\pi\sqrt{LC}}$$

The LC oscillator used in this paper is not based on the logic delay, but on the resonant effect of a passive inductor and capacitor circuit. The physical design of differential LC oscillator shown in figure 4; where the inductor L1 resonates with the capacitor C1 connected to S2, combined with C2 connected to S1.

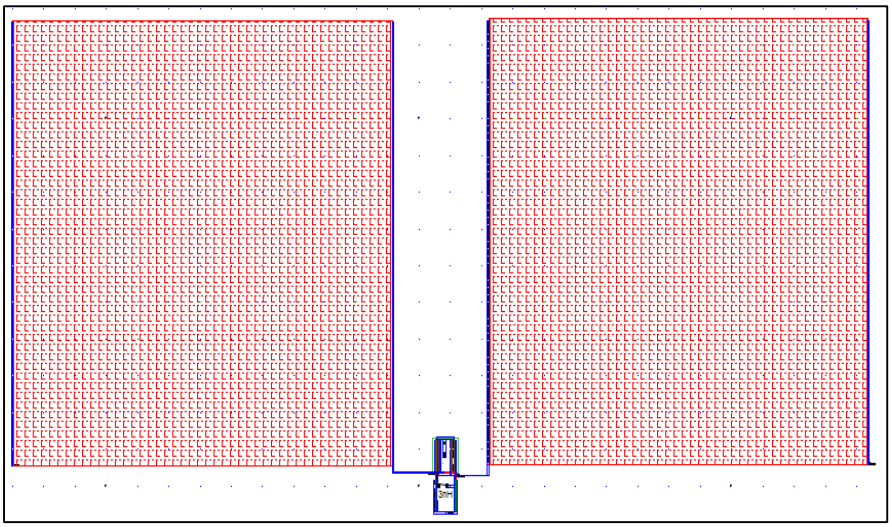

Fig. 4: Physical design of Differential LC Oscillator

For the layout implementation of the LC oscillator, we have to make some calculations as the output frequency is depends on the current of the transistors.

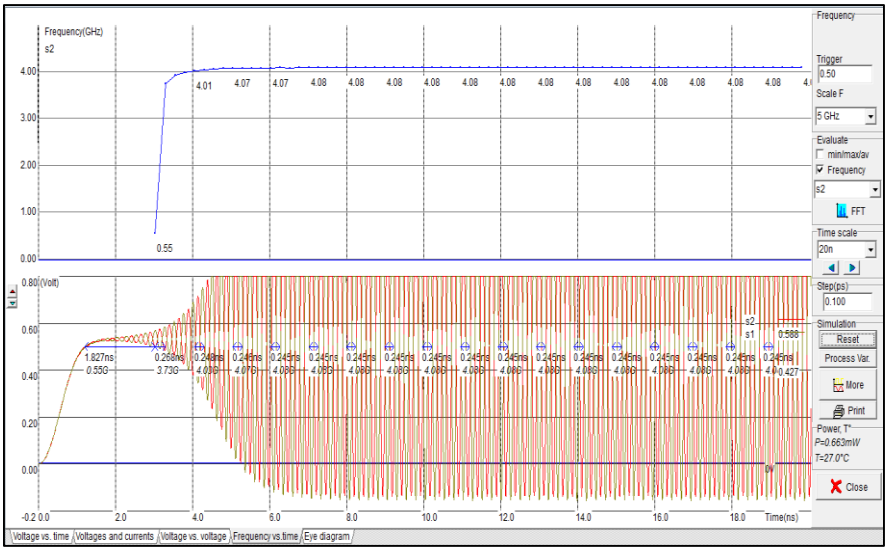

Fig. 5: Frequency vs Time curve

The layout implementation is performed using a virtual inductor L1 and two capacitors C1 and C2 with the specified width and length in table above. Notice the large width of active devices to ensure a sufficient current to charge and discharge the huge capacitance of the output node at the desired frequency. Using virtual capacitors instead of on-chip physical coils is recommended during the development phase. It allows an easy tuning of the inductor and capacitor elements in order to achieve the correct behavior. For the physical design, we used Capacitance = 1 pF each Inductance = 3 nH. For these values of L and C, we are getting the osciilating frequency from the figure as 4.08GHz.

A. Calculated frequency for LC Oscillator

$$fo = \frac{\omega 0}{2\pi} = \frac{1}{2\pi\sqrt{LC}}$$

Where;
L= 3 nH
C= 1.2 pF each
Putting these values in the above equation, we will get;

$$fo = \frac{1}{2\pi\sqrt{3nH * 0.5pF}}$$

= 4.11 GHz.

The calculated frequency for LC oscillator is 4.11GHz. As of the same as Ring oscillator, we can change the L and C values like L=3 nH and C as 1.2 pF, then the calculated oscillating frequency we got is 4.08 GHz.

IV. CONCLUSION

This paper presents the simulation and Implementation of CMOS based Ring and Differential LC oscillators with 45 nm CMOS process. The main air is to find out the simulated frequency and the calculated frequency for application and to understand the stability factor for the oscillators. The Design and Realization of structures include the physical design and simulations. Design, Area and power parameters are optimized by working on physical layout design. The on paper calculated and simulated results should be the same. From our design the results we are getting as;

A. For Ring Oscillator:

Table - 1

Ring Oscillator		
No. of Stages	*Calculated*	*Simulated*
5	*24.64 GHz*	*24.57 GHz*
9	*14.24 GHz*	*13.74 GHz*
11	*11.65 GHz*	*11.20 GHz*
13	*9.86 GHz*	*9.51 GHz*

B. For Differential LC Oscillator:

Table – 2

LC Oscillator		
No. of Stages	*Calculated*	*Simulated*
L= 3nH, C=1pF	*4.11 GHz*	*4.08GHz*
L= 3nH, C=1.2pF	*4.02 GHz*	*4.05 GHz*
L= 3nH, C=2.7pF	*2.5 GHz*	*2.47 Hz*

From the above results, it is clear that the on paper calculated frequency is somewhat equal to the simulated oscillating frequency.

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