

On-Chip Communication for Low Latency on Hybrid NOC Architecture using i-slip Algorithm

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Abstract

As the fabrication technology has been advanced more and more components are implemented on a single platform which makes the communication between this component very difficult unless the proper attention are not given on the communication factor. The system on chip (SOC) has a network version called as network on chip (NOC). Routing algorithm, switching techniques are the main terms in the network-on-chip. Packets between these component can be transfer using the switching techniques. The routing algorithm These communications can be done either by hybrid mesh architecture or bus mesh architecture. In these paper we are going to implement the system, communication where two hybrid mesh architecture are used which has a different algorithm will help us to reduce the latency for the communication for the data. The main purpose of this paper is to reduce the latency of the data communication Here the heavy IP cores are placed in same subsystem and data transfer is carried out with the help of the routing algorithm. Efficient partition and mapping are proposed for the routing algorithm.

Keywords: Hybrid NOC Architecture, X-Y Routing Algorithm, IP Cores, Mesh Architecture, i-slip Algorithm, Latency Factor

I. INTRODUCTION

Semiconductor technology have been increasing very rapidly and technology is also been advance day by day. In the latest trend of the semiconductor technology, the data communication is carried out using the IP that is functionally intellectual property. IP cores are placed on the single platform. By connecting the IP core it will help to develop the complex bus system. Bus system has a different problem such as scalability, and if the IP cores are increased in number, communication of the data will become slow in the bus based system.

NOC maps the IP on a block and transmit data between the IP using network communication. Based bus system is no longer useful for the complex SOC so the network based system are used to overcome the scalability issue. In this paper we purposed bus-mesh architecture for SOC design which will provide the communication of the data having low latency.

Here the IP are placed on the same subsystem which have the high communication affinity and high data traffic.

The main purpose is to reduce the latency required for the data communication, Hot spot problem will get reduce while considering the based architecture. Routers are used to connect the IPs and data will transfer through the routers. These routers will also use to connect to the neighboring router. Design interface is not needed for each IP, which can further reduce the design cost, power consumption.

This paper implements the X-Y router with the i-slip routing algorithm, where the efficient data communication in the SOC as well as on NOC device can take place. Full IP to IP routing capability can efficiently be provided. The following section describe the design challenge in section II, proposed work in section III and conclusion in section IV.

II. DESIGN CHALLENGES

The hybrid system is based on NOC and it is a bus based system. IP cores are placed on same subsystem and they are heavily affiniated .the figure shows the hybrid NOC architecture ,where the different symbols represent the different terms for eg R is the router, S is the subsystem, C denotes the single IP core , B denotes the bridge. If the data transfer takes place from subsystem to network then it will be serves as the slave component and when communication take place between network to subsystem then it will serve as the master component. The main function of the bridge to packetize and deliver them to routers. when data is transferred from network to subsystem it will serves to depacketized them.

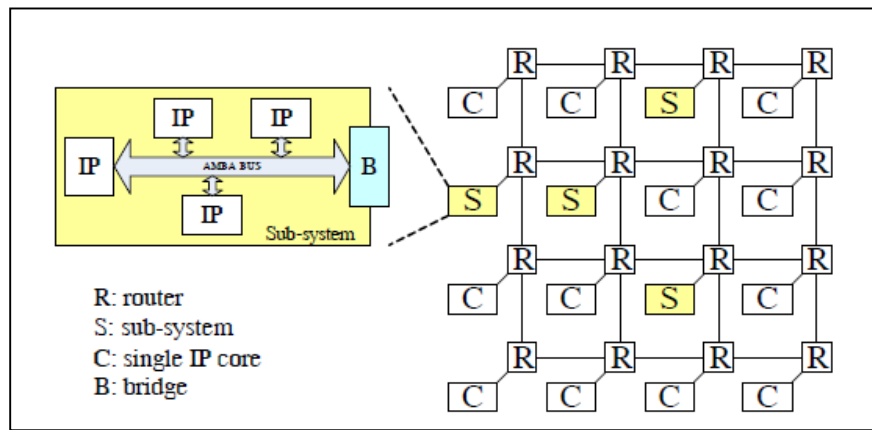


Fig. 1: Hybrid NoC Architecture

A. Bus Latency Formula:

The calculation of the latency of the bus with the single master

$$L_{bus} = (3 - 2U) \cdot N_D \cdot S + \left\lceil \frac{N_D \cdot (1 - S)}{B} + N_D(1 - S) \right\rceil$$

Where N_D is the number of data, S is the rate of single mode transfer, B is the size of burst data and U is the usage of bus. But with more bus masters rather than one then it is given by the next formula given below.

$$L_{single_layer} = N_M \cdot L_{bus}$$

B. NoC Latency Formula:

This section will show the formula for the calculation of the latency of the NOC. the packet transmission latency in NoC includes the delay of router and network interface.

$$L_{NoC} = n \times L_{router} + m \times L_{NI}$$

Where L_{router} is the transmission latency of a router to transmit a fixed size packet, the L_{NI} is the latency of network interface to encode or decode a packet. n and m denote the number of routers and number of network interfaces.

III. PROPOSED WORK

This paper proposed a system where the hybrid mesh architecture is used. Hybrid mesh in which we uses the four by four matrixes. They are two in number. The data is passed through the router .the routers are used which are the basic medium to transfer the data.

The individual mesh of four by four matrix are given the individual naming . with using the different algorithm, the data is been passed through this mesh, which will rout the data will be produce the shortest path and hence which will reduce the overall latency. The two four by four matrix ,the first four by four matrix uses the x-y routing algorithm and output of the first mesh will be given to the other mesh which uses i-slip algorithm. These both routing algorithm are proposed for the achievement of the shortest path and hence overall reduce the latency of the hybrid mesh architecture.

In the first four by four mesh the X-Y router are used. The X-Y router are named such as the data is transfer either in the X direction or in the y direction. They will not transfer the data in the diagonal direction. Logic of the routing algorithm are such that the path will be choose or calculated such that it will take as less time as possible ,hence the latency is get reduce . The X-Y router produce the path instantly and no delay will be produce. The bit transfer is formatted in such a way that it consist of the sixteen bit naming as 15 to 0 bit. The format is specified below.

We have the mesh four by four .name this terminal as A1,A2,A3,A4. This four by four matrix are named such as 0,0;1,0;2,0;3,0; for the first row. Second row is named as 0,1;1,1;2,1;3,1;third row is named as 0,2;1,2;2,2;3,2;and fourth is considered as 0,3;1,3;2,3;3,3;now consider the matrix 0,1 the the address of the X will be given as 0 and the address of the Y is given as 1.like wise it will be considered. The data will pass either X-direction or in y direction. The frame format will be describe by the address of the block. The frame will be describe below.

The frame format will be such that first 8 bit will be the data which has to be transferred from 0 to 7 , then 8 to 10 bits are considered as don't care. 11 and 12 bit will give the address of the Y matrix destination and 13 and 14 bit will specify the destination of X matrix. The 15 bit gives the, form which terminal the input is given. The 15 bit is enable by 1.

The second four by four mesh are routed with the i-slip routing algorithm. In the i-slip algorithm the basic frame format described above is used such that it will search a path where the first origin will be fixed and the routing will be done such that it will compare the destination address of the x address with the fix location and it will search a path. Hence whatever the path is been observed then it will give the output will low latency the searched path will produce a path which will cover a less distance and hence the overall latency will be reduce..

IV. RELATED WORK

Since the hybrid NOC architecture the data is passed from one mesh terminal to another mesh using X-Y and i-slip routing algorithm. The overall latency is reduced when compared. It is been compared with the different paper and hence the latency is found to be reduce. The overall over is carried out in modelsim software. The output of the proposed work is shown below.

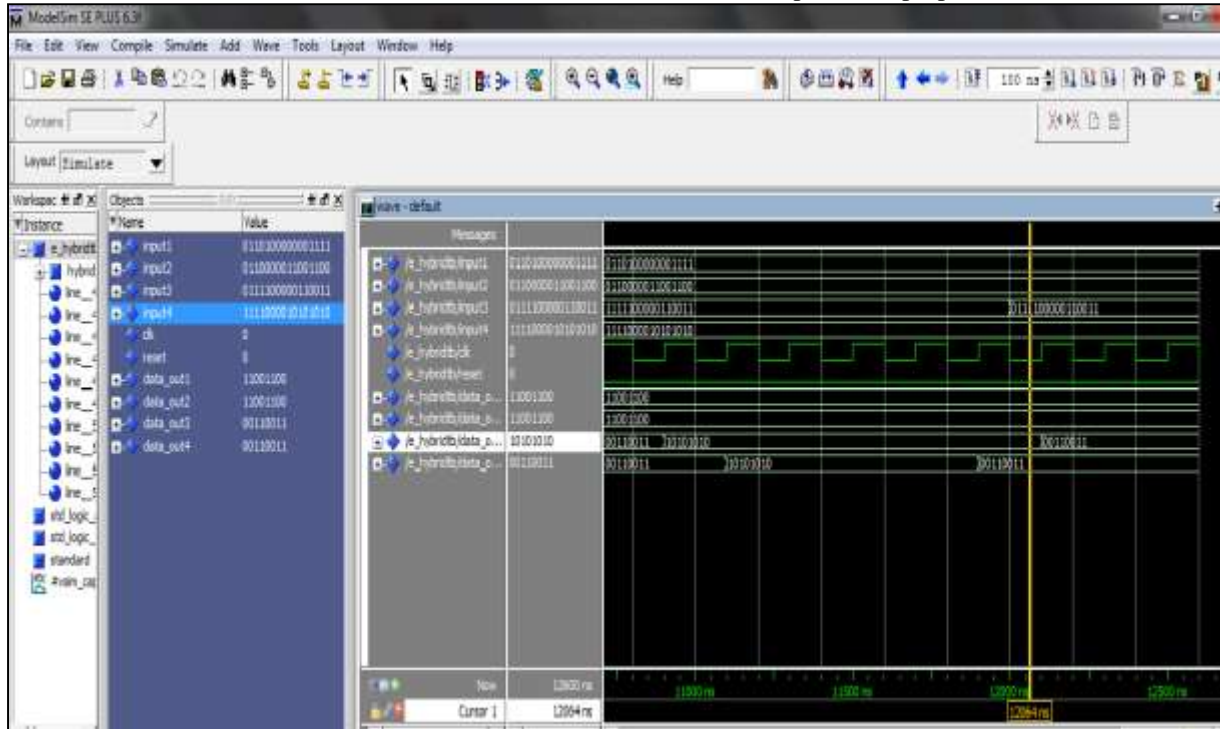


Fig. 2: Screenshot of Proposed Work

V. CONCLUSION

The purposed work of architecture is used to reduce the latency of the data communication. Here we conclude that the using the X-Y routing algorithm on single mesh architecture verify the shortest path. i-slip algorithm on the next mesh verify that it is a fast algorithm while it computes in N-iteration. I-slip algorithm is a starvation free and simple to implement, high throughput. since the data is travelled between two hybrid NOC in proper format, the required logic makes the data communication between the ip's, which is routed by the routing algorithm takes less time and efficiently reduces the latency of the data communication.

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