Comparative Analysis of Interpolation/Decimation FIR Filter Structures for WLAN-b and WLAN-g Applications

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Abstract

The major focus of this paper is to analyze the different realization of Interpolation/Decimation Filter Structures that supports WLAN applications. Based on overall sampling rate (M=12) is used to design the efficient interpolation/decimation FIR filter structure for WLAN-b and WLAN-g applications. Polyphase realization FIR filter is tailored in such a way to reduce the computation complexity of the filter to save the delay with polyphase structure will reduce the power consumption of DDC. Finally the results show that the presented structure consumes less computation compared to other structures considered for analysis.

Keywords: Decimation Filter, Down Sampling, Finite Impulse Response Filter, Multistage and Sampling Rate Conversion

I. INTRODUCTION

In digital signal processing, manufacture spotlight the Digital down Converter (DDC)/Digital up Converter (DUC) as sample rate converters, which is one of the important blocks in every digital communication systems. Hence there is a need for effective realization of sample rate converter to reduce the area and power significantly. The decimation/interpolation filter is one of the basic blocks in DDC/DUC. It performs decimation/interpolation and matched filtering to eliminate the nearby channels and improve the received signal-to-noise ratio (SNR). Their design and operation can affect the performance of the whole system.

The decimation filter finds wide application in both analog and digital systems for the purpose of data rate conversion as well as filtering. It has been widely used in audio, speech processing, radar systems and communication systems. The requirement of efficient decimation filter structure is increasing rapidly for different reasons in the past few decades. This high demand has created interest among researchers and design engineers to develop efficient decimation filter structure with less complexity.

WLAN is a wireless data communication technology, based on IEEE 802.11 standard. It provides high data speed over an extensive range. A wireless local area network (WLAN) is a wireless network that relatives two or more devices using a wireless distribution technique within a partial area. It gives users in its ability to shift around within a local coverage area and tranquil be connected to the network, and can provide a connection to the wider Internet. Make use of a wireless transmission medium.

The essential function of interpolation/decimation is to decrease the sampling rate and to keep the passband aliasing within approved bounds. In this paper we are designing the decimation filter structure for WLAN b and WLAN g standard as per the specification mentioned in the table-1. The sampling rate reduction required for WLAN is 12, which is realized with multistage FIR filter based decimation filter structure which reduces the computational complexity.

Table - 1
Filter Design Specification for WLAN b and WLAN g Applications

<table>
<thead>
<tr>
<th>Parameters</th>
<th>WLAN - b</th>
<th>WLAN - g</th>
</tr>
</thead>
<tbody>
<tr>
<td>Over Sampling Rate</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>Input sampling frequency F_s (MHz)</td>
<td>132</td>
<td>144</td>
</tr>
<tr>
<td>Pass band Edge (MHz)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Stop band Edge (MHz)</td>
<td>12.5</td>
<td>12.5</td>
</tr>
<tr>
<td>Pass band ripple (dB)</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Stop band attenuation(dB)</td>
<td>44</td>
<td>44</td>
</tr>
</tbody>
</table>

The Non-recursive filters have a distinct frequency response but they require large amount of hardware to store the filter coefficients. The recursive filters are simpler in structure, but they do not satisfy the requirements of linear phase filter which are...
very much required for obtaining time aware features like speech and video. Hence an alternate decimation filter structure which consumes fewer coefficients and less power consumption is in high demand.

II. RELATED LITERATURE WORKS

In a polyphase multistage FIR filter with memory saving structure has been studied. The structures are implemented with help of Xilinx system generator [1]. In this paper [2] presents the multiplier less FIR filter structures realization. It describes the total number of adders required for the transposed direct form; polyphase realization and reduced complexity polyphase FIR filter structures with a comparison. In this paper [3] have implemented the polyphase decomposed FIR filters having interpolation and decimation filter structure. For interpolation, direct form realization having direct to fewer registers but in transposed form realization, registers cannot be shered easily. These two realization structures are opposite for decimation factors, to end with implementation results for area, speed, and power for different realizations are compared.

This paper [4] focuses on the design of efficient decimation filter structure realization for GSM Applications. In order to reduce the complexity of the decimation filter structure, FIR filter with decimation factor M is subdivided into multistage with different decimation factors. The results show that the multistage efficient linear phase structure reduces the complexity of the decimation filter structures significantly compared to other structures. This paper presents [5] the implementation of two stage FIR (Finite Impulse Response) decimation filter using system generator and it is distinguished with single stage implementation of FIR filter for WiMAX Application. Basic structure is designed with MATLAB Simulink model and it is converted to Verilog code using Xilinx system generator. It is used to check the hardware kit Virtex- V FPGA components and device utilization reports are generated and tabulated. This paper presents [6] architecture of a high- throughput 4x4 64-QAM MIMO receiver consists of a channel matrix QR decomposition. The recent works MIMO receiver provides low processing jitter and a pipelined architecture scalable to a huge amount of antennas and constellation order.

The first system parameters designed [7] the WiMAX base stations have to be selected. The second system parameter is in which platform having to be used. And third system parameters is on which algorithm have to be selected for some receiver modules such as synchronization, channel estimation and STC decoder. Finally, BS design and implementation on specific platform to achieve meant system performance. This paper presents [8] the design, implementation and tentative validation of a real-time FPGA-based mobile WiMAX baseband transceiver. It also includes a block description of the implemented baseband processing elements for each antenna scheme. A real-time testbed has hosted the three baseband implementations. A dedicated data-capturing edge facilitated their performance comparison in respect to the equivalent Matlab models.

This article [9] describes the VHDL implementation of convolutional turbo code of an OFDM system based on adaptive data rate control of OSI layer according to the WiMAX standard IEEE 802.16. This work described the generation of the convolutional turbo code, in fixed-point and its conversion to VHDL, of an OFDM system based on adaptive control of the data rate physical layer of WiMAX in accordance with the IEEE 802.16. It requires higher capacities, data rates and different operating modes have motivated the development of new generation multi-standard wireless transceivers. A multi-standard design often involves extensive system level analysis and architectural partitioning, typically requiring extensive calculations. In this research, a decimation filter design tool for wireless communication standards consisting of GSM, WCDMA, WLANa, WLANb, WLANg and WiMAX is developed in MATLAB using guide environment for visual analysis [10].

III. VARIOUS STRUCTURES & METHODOLOGY

The Symmetric nature of FIR filter [7] offers the occasion to create realization schemes which significantly to reduce the less computation efficiency and complexity of the decimator/interpolator. Consider the factor M-decimator of which reduces the aliasing problem, filter with the impulse response h[n]. The time domain relation for the filter are expressed by the convolution sum,

\[ v[n] = \sum_{k=0}^{N-1} h[k] x[n - k] \]  

(1)

Where N is the order of the filter.

The decimated signal y[m] is obtained after applying down sampling which is given by,

\[ y[m] = \sum_{k=0}^{N-1} h[k] x[nM - k] \]  

(2)

Fig. 1 represents the cascade of an FIR filter and down-sampler and Fig. 2 shows the direct realization structure of factor-of-M decimator.

![Factor of M-decimator with FIR filter](image)
Comparative Analysis of Interpolation/Decimation FIR Filter Structures for WLAN-b and WLAN-g Applications

**Fig. 2:** Direct Realization of factor-of-M decimator

**Fig. 3:** Efficient realization of factor-M decimator

The efficient structure that realizes equation (2) is depicted in Fig. 3. The down-sampling operation precedes the multiplication and additions, so the arithmetic operations are evaluated at the down sampled rate \( F_s / M \). On comparing FIR and efficient filter realization, the number of multiplication per input sample in the decimator is equal to filter length \( N \). On the other hand the efficient realization structure of FIR filter reduces the number of multiplication per input sample to \( N/M \). This will improve the efficiency of the FIR filter.

### IV. Polyphase Decomposition

A higher-order FIR filter can be realized efficiently in a parallel structure based on the polyphase decomposition of the transfer function. The FIR transfer function is decomposed into \( M \) lower-order transfer functions called polyphase components, which are added together to compose the original overall transfer function.

In general, an \( N \)-length transfer function \( H(z) \) can be decomposed into \( M \) polyphase branches of \( E_0(z), E_1(z), \ldots, E_{M-1}(z) \) and hence the \( H(z) \) can be expressed in the form,

\[
H(z) = \sum_{k=0}^{M-1} E_k \left( z^{-M} \right)
\]

\[
E_k(z) = \sum_{n} h[M(n + k)]z^{-N}, \quad 0 \leq k \leq M - 1
\]

An FIR filter can be implemented as a parallel connection of \( M \) polyphase components, sometimes called polyphase branches or polyphase subfilters, which are added together at the output. A polyphase branch is usually implemented in the direct transversal form as shown in the Fig. 4, a decimator composed of the cascade of an FIR filter implemented as a parallel connection of \( M \) polyphase branches and factor-of-\( M \) down sampler. Here the arithmetic operations are performed at the input sampling rate in the polyphase branches and the down sampling at the filter output.

The number of arithmetic operations can be reduced by applying the third identity, and to get the efficient polyphase realization structure shown in Fig. 5. Here the down sampling operation shifted at the input of the polyphase branches \( E_0(z), E_1(z), \ldots, E_{M-1}(z) \) and the filtering is performed at the sampling rate \( F_s / M \), so that the overall computational complexity of the decimator is reduced by \( M \).

The input sequences to the polyphase branches of Fig. 5 are delayed and down sampled versions of the input signal \( x[n] \). Here the particular input sequence is obtained by down sampling the sequence by \( M \) with the phase offset \( k \), \( k = 0, 1, \ldots, M-1 \). Those sequences can be selected from the input signal \( x[n] \) directly by using the commutative structure with the rotator shown in Fig. 6.
The rotator starts at the starting time \( n = 0 \) and gives the current sample \( x[0] \) to \( E_0(z) \) and the next sample \( x[1] \), at the time \( n=1 \), goes to \( E_{M-1}(z) \). The rotator continues in the same manner by moving to the left. Here the rotator operates at the rate of high-rate input signal \( x[n] \), where filtering in the polyphase branches is performed at the rate of the low-rate signal \( y[n] \).

**V. PROPOSED METHODOLOGY - EXAMPLE FOR WLAN-B**

The significant savings in computational requirements can be achieved when the sampling rate reduction is accomplished in multistages. The decimation factor \( M \) is factored into a product of integer to get the multistage decimator. In this proposed methodology, the advantages of the structures presented earlier are to be considered, to develop the structure which can reduce the computational complexity than the existing system and conventional FIR filter structure. For this proposed method the multistage design can be analyzed using the two-stage decimation with the overall conversion factor of \( M \).

The computational efficiency is determined by the number of multiplications per input sample (MPIS) for the decimator and the number of delays (memory elements). Alternatively the computational efficiency can be expressed as the number of multiplications per second. 

Single-stage FIR filter based decimator structure for \( M \)

For the single-stage decimator, the polyphase decimator for the factor-of-\( M \) is realized according to Fig. 7, and then the arithmetic operations are calculated at the lower sampling rate. For this design the multiplication rate \( R_{\text{m\_dec}} \) is given by the equation (4) and this single-stage decimator structure for \( M \) is shown in Fig. 7.

\[
R_{\text{m\_dec}} = N \times F_s = F_s \times N/M
\]

Example for wlan b

Consider factor-of-12 decimator which converts the input sampling rate \( F_s = 132 \text{MHz} \) to the output sampling rate of \( F_s = 11 \text{MHz} \), specified in table 1 with the filter design parameters \( F_s = 10 \text{MHz} \), \( F_s = 12.5 \text{MHz} \), \( \delta_p = 0.5 \text{ dB} \) and \( \delta_s = 44 \text{ dB} \)

The decimation factor \( M=12 \) is expressed as a product of two integer, ie. \( M=4\times3 \), instead of single-stage decimation. Here the decimation performed in two steps expressible as a product of two integer \( M=4\times3 \) can be determined, which is shown in figure 8. The single-stage equivalent of Fig. 9 is obtained by using the third identity to the cascade of the factor-of-4 down-sampler and filter.
In order to reduce the multiplication rate the realization of proposed two-stage FIR based decimator structure designed using polyphase for M=12 is shown in Fig. 8.

The input signal is decimated by 4 in the first stage and in the second stage by 3. The role of filters $H_1[z]$ and $H_2[z]$ is to provide the overall design requirements specified for the decimator are met. Hence the overall decimator characteristics are the design goal when specifying the particular design requirements for $H_1[z]$ and $H_2[z]$.

**VI. RESULTS & COMPARISONS**

The results found that the different types of realization structure in different multistage solutions are given below. It shows how to minimize the multiplication per input sample (MPIS) and reduced the delay and adder element. Finally these structures are compared to reduce the complexity and improve the computational efficiency.

Solution for single-stage realization structure for M=12

For the single-stage equivalent decimation filter structure, FIR filter of the length $N=90$ meets the design requirements specified in the above example.

$$R_{m_{\text{dec,}H}} = 45 \times 11000000 = 495,000,000$$

Number of delay elements required = 89

Solution for two-stage realization structure for $M_1=4$ and $M_2=3$

The specifications for $H_1[z]$ are met with an optimal FIR filter of the length $N_1=21$ and an optimal FIR filter of the length $N_2=24$ meets the specifications for $H_2[z]$ to match the design requirements specified in the above example.

Multiplication rate for two-stage decimation structure is,

$$R_{m_{\text{dec,}H_1}} = 10 \times 33000000 = 330,000,000$$

$$R_{m_{\text{dec,}H_2}} = 12 \times 11000000 = 132,000,000$$

The total multiplication rate of two-stage decimation structure is,

$$R_{m_{\text{dec}}} = 462,000,000$$

Number of delay elements required = 43

Similarly same procedure is followed for WLANg to calculate the multiplications per input samples (MPIS), number of delay elements and number of adder elements are required. Finally the results also same for WLANg because of design specification is same.

### Table - 2

<table>
<thead>
<tr>
<th>Realization Method</th>
<th>Direct Implementation</th>
<th>Efficient Direct Implementation</th>
<th>Linear Phase Implementation</th>
<th>Efficient Linear Phase Implementation</th>
<th>Polyphase Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Single - Stage Realization with M=12</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Length of the Filter</td>
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<td>90</td>
<td>90</td>
<td>90</td>
<td>90</td>
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<tr>
<td>MPIS</td>
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<td>979000000</td>
<td>5874000000</td>
<td>4950000000</td>
<td>979000000</td>
</tr>
<tr>
<td>Number of Delays Required</td>
<td>89</td>
<td>89</td>
<td>89</td>
<td>89</td>
<td>88</td>
</tr>
<tr>
<td>Number of Adders Required</td>
<td>89</td>
<td>89</td>
<td>89</td>
<td>89</td>
<td>88</td>
</tr>
<tr>
<td><strong>Proposed Two - Stage Realization with M_1=4 and M_2=3</strong></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Length of the Filter</td>
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<td>45</td>
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<tr>
<td>MPIS</td>
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<td>957000000</td>
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<tr>
<td>Number of Delays Required</td>
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<td>43</td>
<td>43</td>
<td>42</td>
</tr>
<tr>
<td>Number of Adders Required</td>
<td>43</td>
<td>43</td>
<td>43</td>
<td>43</td>
<td>42</td>
</tr>
</tbody>
</table>

**VII. CONCLUSION**

The design of efficient multistage FIR filter structure for decimation factor M=12 has been proposed and presented. The results shows that the computation efficiency, number of delays and complexity have been reduced significantly compared to other structures in the FIR filter design.
REFERENCES


[7] Qing Wang, Yonghua Lin, Jianwen Chen, Da fan and Ling Shao, “Design and implementation WiMAX transceiver on multicore platform,” IBM china research lab and Tsinghua university Beijing, P.R.China,100193.

