Design and Synthesis of 16 bit Adaptive Digital Filter Architecture

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Abstract

Filtering data in real-time requires dedicated hardware to meet demanding time requirements. If the statistics of the signal are not known, then digital filtering algorithms can be implemented to estimate the signals statistics iteratively. Modern field programmable gate arrays (FPGAs) include the resources needed to design efficient filtering structures. This research aims to combine efficient filter structures with optimized code to create a system-on-chip (SoC) solution for various digital filtering problems. LMS algorithms have been coded in VHDL. The designs are evaluated in terms of filter throughput, hardware resources, and speed performance and to evaluate the mean square error of 16 adaptive digital filters.

Keywords: LMS, FPGA, VHDL, Soc

I. INTRODUCTION

This paper is to explore the use of embedded System on Chip (SoC) solutions that modern Field Programmable Gate Arrays (FPGAs) [1] offer. Specifically, it will investigate their use in efficiently implementing digital filtering applications, [2] Different architectures for the digital filter will be compared with LMS algorithms implemented in the FPGA fabric only, to determine the optimal system architecture. and design and synthesized of 16bit LMS Adaptive Filter with and without using DA and to evaluate mean square error of 16 bit adaptive filter with parameter convergence factor 0.5 and filter length 16 bit and no of iteration 1000.

Recently mobile communication systems require size reduction, high levels of integration and fewer surface-mounted devices as to achieve low cost, robust and highly efficient operation of the system. FPGA technology provides benefits of low cost and of high integration with neighboring circuits. [3] Best architecture give the better solution for system chip level. The electronics industry has achieved an excellent growth over the last few decades, mainly due to the rapid advances in integrated technologies and FPGA Technology. The use of integrated circuits in high performance computing, telecommunications, and consumer electronics has been growing at very fast pace in digital domain. Better architectures of digital filter give the best output of filtering of data.[4] The purpose of this thesis is to explore the use of embedded System on Chip (SoC) solutions that modern Field Programmable Gate Arrays (FPGAs) offer. Specifically, it will investigate their use in efficiently implementing digital filtering applications, Different architectures for the digital filter will be compared with LMS algorithms implemented in the FPGA fabric only, to determine the optimal system architecture Modern computational power has given us the ability to process Tremendous Amounts of data in real- time. DSP is found in a wide variety of Applications, such as: filtering, speech recognition, image enhancement, and data Compression, neural networks; as well as functions that is unpractical for Analog implementation, such as linear- phase filters Signals from the real World are naturally analog in form, and therefore must first be discretely Sampled for a digital computer to understand and manipulate. The signals are discretely sampled and quantized, and the data is represented in binary format so that the noise margin is overcome. This makes DSP algorithms insensitive to thermal noise. Further, DSP algorithms are

Predictable and repeatable to the exact bits given the same inputs. [6]This has the advantage of easy simulation and short design time. Additionally, if a prototype is shown to function correctly, then subsequent devices will also .There are many advantages to hardware that can be reconfigured with different programming files.[7] Dedicated hardware can provide the highest processing performance, but is inflexible for changes. Reconfigurable hardware devices offer both the flexibility of computer software, and the ability to construct custom high performance computing circuits the hardware can swap out configurations based on the task at hand, effectively multiplying the amount of physical hardware available.

II. ADAPTIVE DIGITAL FILTER

An adaptive filter is a filter that self-adjusts its transfer function according to an optimization algorithm driven by an error signal. Because of the complexity of the optimization algorithms, most adaptive filters are digital filters. By way of contrast, a non-adaptive filter has a static transfer function. Adaptive filters are required for some applications because some parameters of the desired processing operation (for instance, the locations of reflective surfaces in a reverberant space) are not known in advance. The adaptive filter uses feedback in the form of an error signal to refine its transfer function to match the changing parameters. Generally speaking, the adaptive process involves the use of a cost function, which is a criterion for optimum performance of the filter, to feed an algorithm, which determines how to modify filter transfer function to minimize the cost on the next iteration. As the power of digital signal processors has increased, adaptive filters have become much more common and are now routinely used in devices such as mobile phones and other communication devices, camcorders and digital cameras, and medical monitoring equipment. In practice, signals of interest often become contaminated by noise or other signals occupying the same band of frequency. When the signal of interest and the noise reside in separate frequency bands, conventional linear filters are able to extract the desired signal. However, when there is spectral overlap between the signal and noise, or the signal or interfering signal's statistics change with time, fixed coefficient filters are inappropriate.

This situation can occur frequently when there are various modulation technologies operating in the same range of frequencies. In fact, in mobile radio systems co- channel interference is often the limiting factor rather than thermal or other noise sources. It may also be the result of intentional signal jamming, scenario that regularly arises in military operations when competing sides intentionally broadcast signals to disrupt their enemies' communications. Furthermore, if the statistics of the noise are not known a priori, or change overtime, the coefficients of the filter cannot be specified in advance. In these situations, adaptive algorithms are needed in order to continuously update the filter coefficients.

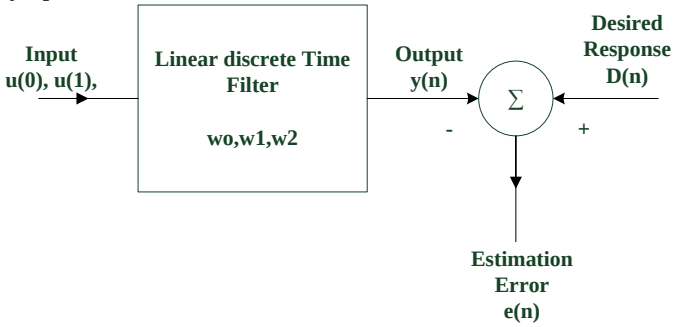


Fig. 1: Block Diagram for the Adaptive Filter

III. LEAST MEAN SQUARE ALGORITHM: THE LEAST MEAN SQUARE (LMS) ALGORITHM

Least Mean Square Algorithm: The Least Mean Square (LMS) algorithm, introduced by Widrow and Hoff in 1959 is an adaptive algorithm, which uses a gradient-based method of steepest decent LMS algorithm uses the estimates of the gradient vector from the available data. LMS incorporates an iterative procedure that makes successive corrections to the weight vector in the direction of the negative of the gradient vector which eventually leads to the minimum mean square error. Compared to other algorithms LMS algorithm is relatively simple; it does not require correlation function calculation nor does it require matrix inversions.

Consider the Nth order of FIR(Finite Impulse Response) digital filter with input signal vector S(k) and N-taps Coefficients vector W(k) can be expressed as;

$$S(k) = [s(k), s(k-1)\ldots s(k-n+1)]T \quad (1)$$

And

$$W(k) = [w0(k), w1(k)\ldots WN-1(K)]T \quad (2)$$

An output signal of FIR digital filter can be expressed as

$$Y(k) = ST(K)W(K)=FTAT(K)W(K) \quad (3)$$

Defining an address matrix A (k) and scaling vector F as,

$$A(k)=[\blacksquare(b0(k)\&\cdots\&b0(k-N+1)@\vdots\&\ddots\&\vdots@b\_(B-1(k))\&\cdots\&b\_(B-1(K-N+1)))] \quad (4)$$

And

$$F = [-20 , 2,.2-(B-1)]T \quad (5)$$

Where B is input signal world length, the relationship between input signal and address matrix can be shown as follows;

$$S(k) = [b0(k),b1(k),\ldots..bB-1(K)]F \quad (6)$$

From eq. (4) the address vector will be defined as;

$$Avid(k) = [bi(k),bi(k-1),\ldots\ldots,bi(k-N+1)]T$$

$$i=0, 1,., B-1, \quad (7)$$

Digital equalization for PRML channel uses least mean square (LMS) algorithm in order to update filter coefficient. The equation for coefficient updating of LMS algorithm [2-9] can be expressed as.

$$W(k+1) = W(k) + 2\mu e(k)S(k) \quad (8)$$

Hence multiply the both side of Eq.(8) by AT(K) will give

$$AT(K)W(K+1) = AT(k)[W(k)+2\mu e(k)S(k)] \quad (9)$$

Replace S (K) =A (K)F into Eq.(9) will be

$$AT(K)W(K+1)=AT(K)[W(K)+2\ \mu e(k)A(K)F] \quad (10)$$

The error signal e(k) can be obtained by;

$$e(k)= d(k)-y(k) \quad (11)$$

Where d (k) is a desired signal

The adaptive function space (AFS) is defined as

$$P(k)= AT(K)W(K)=[P0(K),\ldots\ldots\ldots\ldots..PB-1(K)] \quad (12)$$

$$\text{And } P(K+1) =AT(K)\ W\ (K+1) = [P0(K+1),\ldots\ldots\ldots\ldots..PB-1(K+1)]T \quad (13)$$

The ith elements of p (k) and p(k+1) are partial products that related to address vector AVi(K)

Which is ith row vector of AT(k).Also, time index of P(k) and P(k+1) correspond to W(k) and W(k+1) respectively. There are 2N partial product for the Nth order input signal vector p(k) and product for the Nth order input signal vector .P(k) and P(K+1) include B elements selected by B address vectors substituting Eq.(12) and Eq.(13) to Eq.(10), will be obtained

$$P(K+1)=P(k)+2\mu e(k)AT(k)A(k)F \quad (14)$$

The output signal can be represents as.

$$Y(k= FTP(k) \quad (15)$$

Assume the input signal is white noise with zero mean unit variance. An expectation value of AT (K) A(k)F becomes

$$E[AT(K)A(k)F=.25NF \quad (16)$$

Replace AT(K) A(k)F in Eq.(14) with Eq.(16), also Eq.(14) is simplified to

$$P(k+1) = p(k)+0.5\mu e\ (k)Ne(k)F \quad (17)$$

The term 0.5 μ N in Eq (17) can be treated as a constant, inter power of two. Therefore, it is possible to implement hardware without multipliers. Also, it can be obtained multiplier less adaptive digital filter with LMS adaptive algorithm.

IV. FLOW GRAPH OF LMS ADAPTIVE ALGORITHM

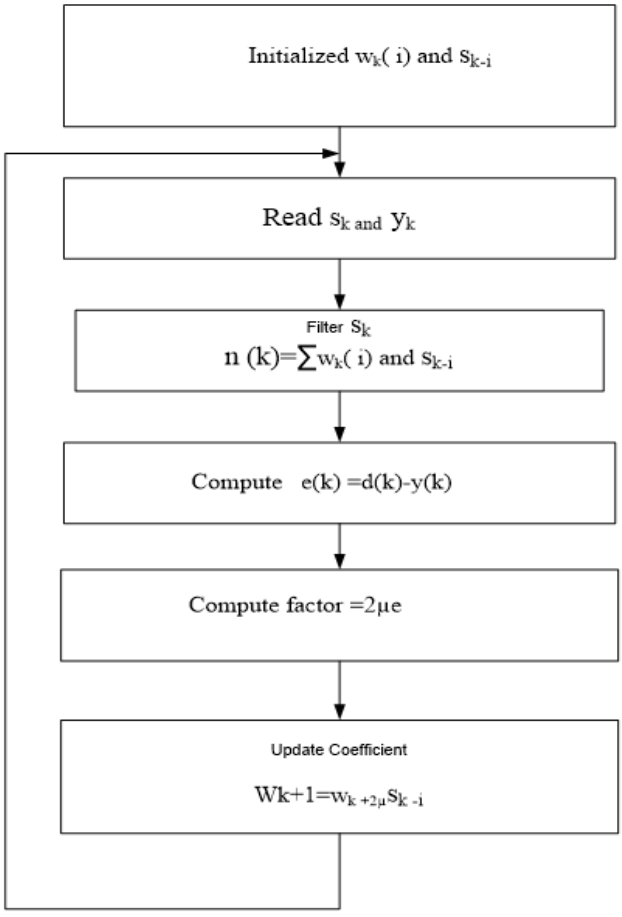


Fig. 2: Design Flows of LMS Adaptive Filter

V. HARDWARE ARCHITECTURE FOR ADAPTIVE DIGITAL FILTER BASED DA

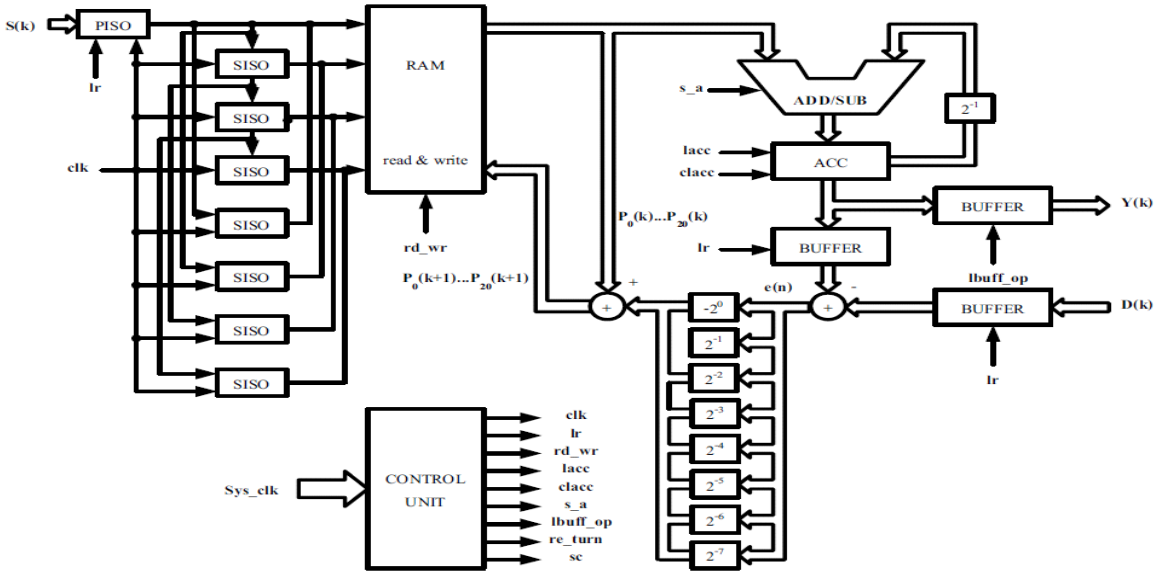


Fig. 3: hardware architecture for adaptive digital filter based DA

A. Working of 16 bit Adaptive digital Filter based DA Architecture:

An architecture for hardware implementation of adaptive filter uses distributed Arithmetic (DA).which is one method often preferred since its eliminates the need for hardware multiplier and is capable of implementing high order filters with very high throughput .

Distributed Arithmetic realization of LMS adaptive digital filter .the major design hardware components consist of PISO (parallel in serial out shift register), SISO (serial in serial out shift register), buffer, scaling, accumulator ,adder, subtract or, update new partial product circuit RAM and control unit .therefore the hardware architecture can be describe by 6 step as follows:

- A/D is controlled by signal SC, will convert analog signal s(t) to digital signal s(k).hence signal lr will be loaded to PISO and signal clk will be shifted each bit of data .data that shifted each bit of SISO by same signal clk.
- Output of PISO and each SISO can be divided to two groups, one group used for RAM addressing. In the same time another used for prepare data to repeat RAM addressing after input signal shifted already.
- For the first time of RAM addressing. Output of RAM will be added to scaled value from ACC using scaling accumulator that controlled by signal s a result will be loaded to ACC by signal lacc. In the time signal d_wr that used for RAM reading will be active.
- Repeat in step 3, output of RAM will be subtracted from scaled value from ACC. result will be loaded to first buffer by signal lr, then signal clacc will clear ACC and signal lbuff_op will be loaded to second buffer for converting digital signal y(k) to analog signal y(t) by D/A.
- Error signal e(n)can be found by difference between desire signal d(k) and output y(k),the error signal will be passed to update new passed to update new partial products circuit that contained with bank of shift register to calculate value 0.5ne(k) .
- Same address by new partial product p(k+1) are old partial product p(k) added with result in step 5.in this time signal d_wr that used for RAM reading will be active ,and repeat in step 1-6 respectively.

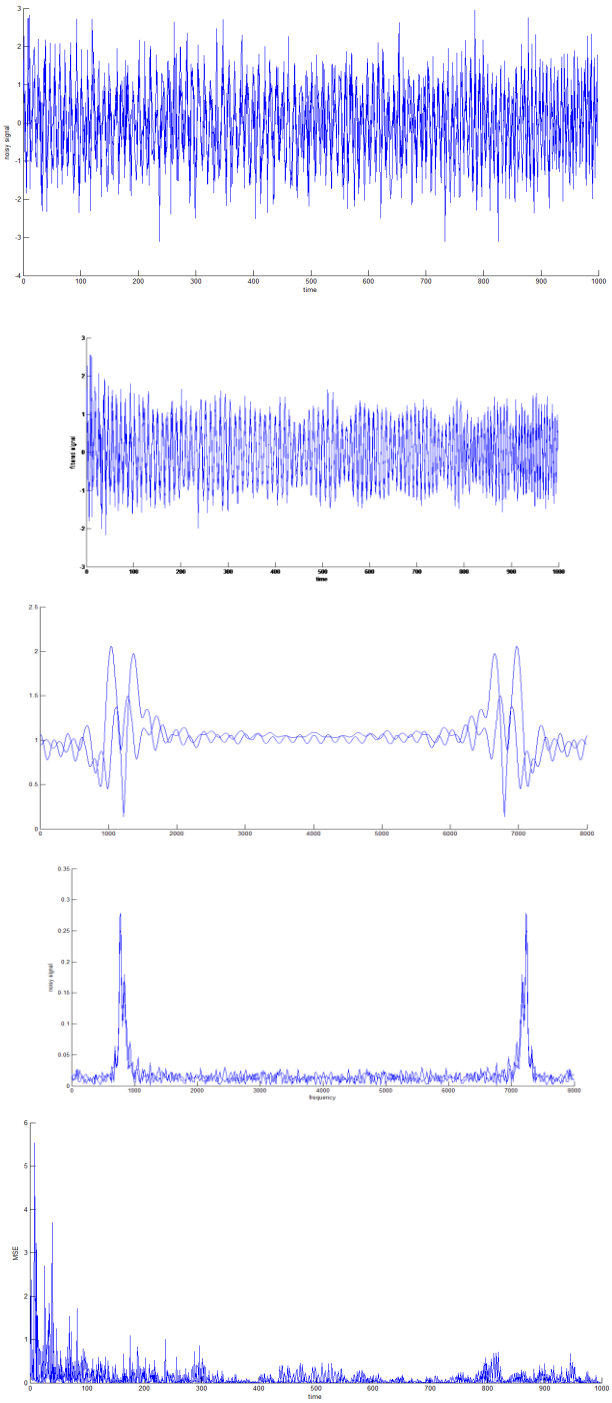
VI. SIMULATION AND SYNTHESIS RESULT (E) THE COMPARISON OF THE PERFORMANCE PARAMETERS

Table – 1
Simulation and Synthesis Result (e) The comparison of the performance parameters

Performance parameter	*8bits Adaptive Digital Filter*	*16 bit LMS Adaptive Digital Filter*	*16 bit adaptive filter using DA*
Memory bits	*320*	*386out of 4646*	*1out of 4 25%*
Memory %Utilization	*5%*	*386out of 4646 8%*	*1out of 72000 1%*
LCs	*506*	*585 out of 9312*	*1of 204000*
LC% Utilized	*87%*	*585 out of 9312 6%*	*1out of 4 25%*
No of 4 input LUTs	-	*585 out of 9312 6%*	*1of 204000*
No of IOs	-	*319 out of9312 6%*	*7*
No of bonded IOBs	-	*67*	*6*

This paper presents the development of algorithm, architecture and Implementation for speech processing using FPGAs. The VHDL code in RTL compliant and works for using Xilinx tools. Adaptive filter is a filter that varies in time, adapting their coefficients according to some reference using LMS algorithm. We are often faced with the problem of estimating an unknown random signal in the presence of noise. This is usually accomplished so as to minimize the error in the estimation according to a certain criterion. This leads to the area of adaptive filtering**.**

VII. DISPLAY THE TIME DOMAIN OF THE UNFILTERED INPUT SIGNAL:



Final Mean square Error = 0.1598.
SNRf = 9.0459

A. Conclusion and Future Work

1) Timing Summary:
Speed Grade:-3
Minimum period: 1.046ns (Maximum Frequency: 956.023MHz)
Minimum input arrival time before clock: 0288ns
Maximum output required time after clock: 0609ns
Maximum combinational path delay: No path found.
2) Timing Details:
All values displayed in nanoseconds (ns)
Clock period: 1.046ns (956.02MHz)
Total number of Path/:3/3
Delay: 1.046ns (levels of logic=0)

Mean square Error 16 bit of LMS Adaptive Filter:
Convergence factor =0.5
Filter length=16
No of Iteration =1000

B. Future Work

High level design languages for programmable logic could help to ease the design flow of difficult algorithms. However, many are still in early stages and have trouble inferring device specific components, such as microprocessors. Evaluating these new languages and their integration with embedded microprocessors, would be useful. Many times the decision to use an embedded microprocessor focuses on the power consumed and logic cells saved. Therefore, framework for determining the amount of equivalent logic cells recovered for a given function on the microprocessor is needed

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