

Dynamic Power Reduction in NOC by Encoding Techniques

Shivaraj MN

PG Student

*Department of Digital Electronics and Communication System
VIAT, VTU, CPGS, Bengaluru Region, Muddenahalli,
Chikkaballapur, Karnataka, India*

Ravi H Talawar

Assistant Professor

*Department of Digital Electronics and Communication System
VIAT, VTU, CPGS, Bengaluru Region, Muddenahalli,
Chikkaballapur, Karnataka, India*

Abstract

As technology improve the size will be reduced, and the power dissipated by the links of a network-on-chip (NoC) is starts to participate with the power dissipate by the other element of communication system, for example the routers and the network interfaces (NIs). We design an set of data encoding technique by different schemes to decrease the power dissipation by an links of NoC, which optimizing the on-chip communication system not only in terms of performance but also in terms of power. The idea presented in this paper is base on encoding the packets before they are inserted in to the network in such a way as to minimize both the switching action and the coupling-switching action in the NoC's link which represent the main factor of power dissipation. These schemes were universal and transparent with respect to the construct NoC fabric that means this application will not require any change in the router and link of architecture. These will be carried in both artificial and real traffic scenario. These effective of the proposed scheme will tolerate to save the energy consumption and power dissipation without changing the performance degradation and with less area consumption in the NI.

Keywords: switching action, encoding, network-on-chip (NoC), low power, router, Network interfaces (NIs)

I. INTRODUCTION

Moving towards silicon technology node to the next results faster and more efficient gates but slower because there is a more power hungry wires. More than 50% of total dynamic power is dissipate in interconnection in current processor, and this was expected to increase more over in the next several years. Global interconnect length does not scale with smaller transistors and local wires. Chip size remains relatively constant because the chip function continues for instance the RC delay increases exponentially. The RC delay in a 1-mm worldwide wire at the smallest pitch is superior to the intrinsic delay of a two-input NAND fan-out. If the raw computation horsepower seems to be un-limited, thanks to the ability of instance more core's in a single silicon chip, scalable issue occur, due to making an efficient and reliable communication among the increasing number of core's, become the real problem. The NOC invent is documented as the most feasible way to tackle with scalable and variability issue that characterize the ultra-deep sub-micron-meter.

Now a days in the on-chip communication issue is relevant, in some of the case more relevant than commutating related issue. The communication sub-system more and more impacts the usual designed objective, and also includes cost (i.e., area of silicon), performances, dissipation of power, consumption of energy and reliability. As technology improves the size is reducing and more fraction of total power is budget of the complex in more core of the system-on-chip (SoC) this is because of communication sub-system.

Here we attention on the technique aim to minimize power dissipation by a network link. The power dissipation in the network is relevant as that dissipation by NIs, routers and it is giving that ordinary to increase the technology scale. We are representing the set of encoding schemes for data which is in binary formate, and it is operated at flit level, and an end-to-end basis, this allows us to minimize the switching action and coupling switching action at the link of an direction is traverse by a packet. This encoding schemes, were transparent by respect to router execution, and they are presented, discussed in both algorithmic-level and architectural level, it is assessed via the simulation in the artificial, real traffic scenario. These analysis gives an different aspects, metrics design, it include area of silicon, energy consumption and dissipation of power. From the results we can conclude that with these proposed encoding schemes that power will save and also energy will be save without changing any major degradation in the performance in the NIs.

II. MOTIVATION AND RELATED WORK

The accessibility of chips is growing every year. In next few years, the accessibility of cores with 1000 cores is foreseen. Since the focus of this paper is to decrease the power dissipation by link which decreases the dynamic power, here we are going review the works in the area and link power reduction. Also these will include some technique. They are, use of shielding to increase line-to-line space and repeater insertion. So above technique have large area consumption. One method is the data encoding

technique, its mainly focus is to reduce the link power. The encoding technique's is categorize in to two group. In 1st group we are going to decrease the power by the self-switching action of the each bus line and avoid the dissipation of power by coupling switching action.

These work concentrate on the different component of the inter connection network such as NIs, router, and link. Because these will reduce power dissipation by an link, in this paper, we are going to brief the review some works in the region of link power reduction. These include the technique that make use of shielding, which increase line-to-line space and repeater inserted. They all increases the silicon chip area. These encode scheme is an additional technique that is employed to reduce dissipation of power in link. The data encoding technique has been classified in to two class. In the first class, encoding technique concentrate on reducing the power due to self-switching action of separate bus line while ignoring an power dissipation due to their coupling-switching action. In these class, bus invert (BI) and INC-XOR have been proposed for these case that casual random data pattern is transmitté through the lines. On the other hand, gray code, T0, working-zone encoding, and T0-XOR were suggest for the case of correlation data pattern. Application particular approach have also been proposed

This class of encoding will not be appropriate to be applied in the deep sub-micron meter technological node where the coupling capacitance constitute an most important part of the total inter-connect capacitance. This will cause the power consumption due to the coupling-switching action to become a big fraction of the total power consumption in the links, that making the aforementioned techniques, which ignore such contributions, inefficient. The works in the second class concentrate on reducing power dissipation through the reducing the coupling-switching action. Among these schemes, the switching action is reduced by using many additional control lines. For example, the data bus width grows from 32 to 55. The techniques proposed in have a smaller number of control lines but the complexity of their decoding logic is high. The technique described as follows: first, the data are both odd inverted and even inverted, and afterwards transmission is perform using these kind of inversion which reduce more switching action. The coupling switching action it is reduced, this is compared with another, so we use a simple decoder although achieving a higher activity reduction.

The scheme presented is to reduce the coupling switching action. In this method, encoder count the number of Type I (Table I) transitions with a weighting coefficient of one and the number of Type II transitions with the weighting coefficient of two. If the number is larger than half of the link width, the inversion will be performed. In addition to the complex encoder, the method only works on the patterns whose full inversion leads to the link power reduction while not considering the patterns whose full inversions may lead to high link power consumption. So the link power reduction achieved through this technique is not as large as it could be. This scheme was also based on the hop-by-hop technique.

In another coding technique presented in, bunches of four bits are encoded with five bits. The encoded bits were isolated using shielding wires such that the occurrence of the patterns "101" and "010" were prevented. This way, no simultaneous Type II transitions in two adjacent pair bits are induced. This technique effectively reduces the coupling switching activity. Although the technique reduces the power consumption considerably, it increases the data transfer time, and, hence, the link energy consumption. This is due to the fact that for each four bits, six bits are transmitted which increases the communication traffic. This technique was also based on the hop-by-hop approach.

III. OVERVIEW OF THE PROPOSAL

The fundamental idea of the proposed technique is, the packet are transferred via the network after that the bits are encoded. This technique will help to decrease the switching action and coupling switching action in the link of network traversed by the packets. This self-switching and coupling switching movement are responsible for the link power dissipation. Here we are going to refer to end-to-end scheme. Based on the end to end scheme we are having a improved advantage. The advantage is a pipeline nature of the switching technique. Since same sequence of all the packets passes through all the links of the routing path. The NI may provide the same power saving for all the links. The advanced scheme, an encoder and decoder block are added to the NI. The encoder encode all the going bits of the packets at the other side the header bit such that the power dissipate by the inner router and point to point link is decrease.

IV. PROPOSED ENCODING SCHEMES

The main goal of this encoding scheme is to reduce the power dissipation by decreasing the coupling transition performance on the link of the inter connection network. In this they are classified 4 types of coupling transitions. A type-I occur when one of the line is switch and remaining one is unchanged. A type-II occurs when one of the lines switches from low to high and another is switch from high to low. A type-III occur both the line switches at the same time. A type-IV occurs when both the lines are remains unchanged. The coupling switching action (T_c) is defined as a weight sum of different type of coupling transition contribution There-fore

$$T_c = K_1 T_1 + K_2 T_2 + K_3 T_3 + K_4 T_4$$

Where T_i is the average number of Type I transition and K_i is its corresponding weight.

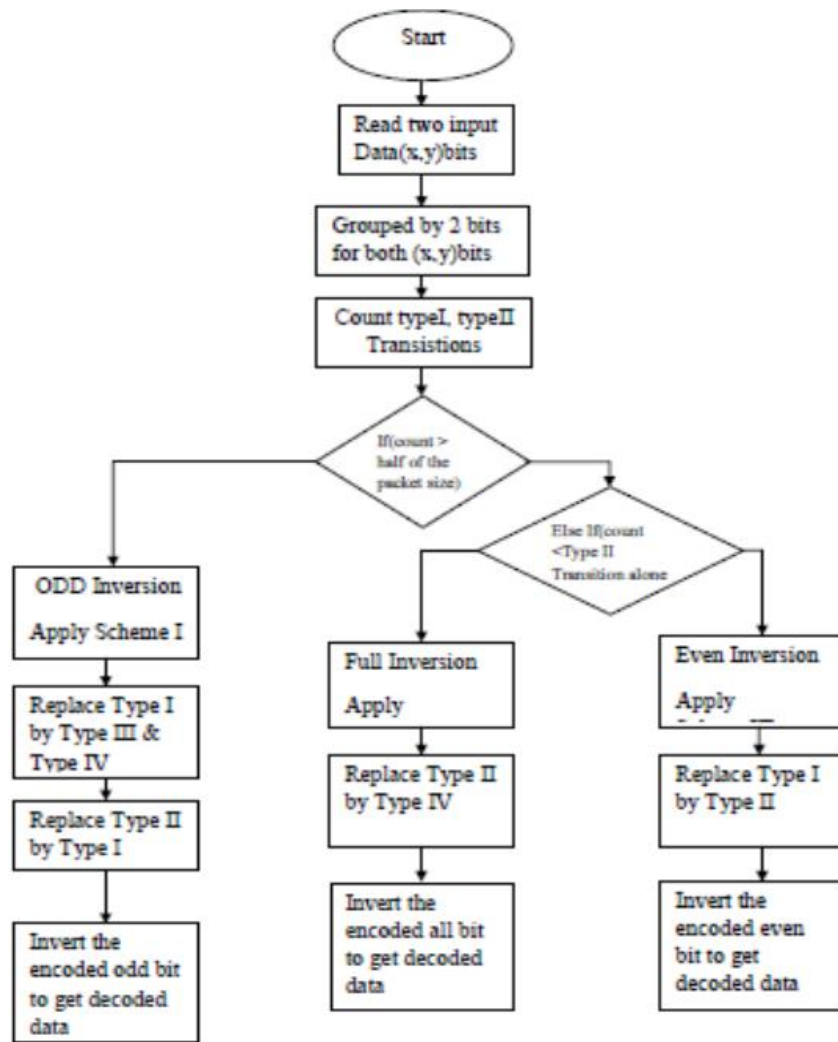


Fig. 1: Flow chart of Proposed Encoding technique

A. Scheme I

In scheme 1, our main goal is to decrease the number of Type-I transition and Type-II transition. Type-I transition is converted into Type III and Type IV transition and Type II transition is converted into Type I transition. This scheme compares the two data's based on reducing the link power reduction by doing odd inversion or no inversion operation with the help of Table-1

Time	Normal			Odd Inverted		
	Type I			Types II, III, and IV		
$t-1$	00, 11	00, 11, 01, 10	01, 10	00, 11	00, 11, 01, 10	01, 10
t	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			11, 00		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			10, 01		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			01, 10, 00, 11		

Table 1: Effect of Odd inversion on change of Transition Types

Time	Normal			Even Inverted		
	Type I			Types II, III, and IV		
$t - 1$	01, 10	00, 11, 01, 10	00, 11	01, 10	00, 11, 01, 10	00, 11
t	00, 11	10, 01, 11, 00	01, 10	10, 01	00, 11, 01, 10	11, 00
	T1*	T1**	T1***	Type II	Type IV	Type III
$t - 1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			00, 11		
$t - 1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			01, 10		
$t - 1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			10, 01, 11, 00		

Table 1: Effect of Even inversion on change of Transition Types

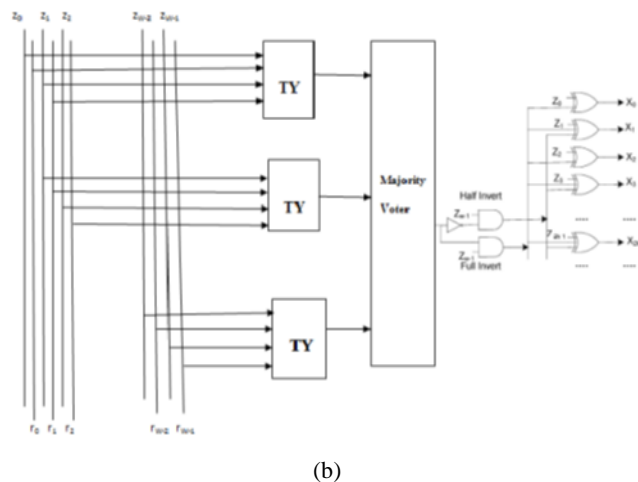
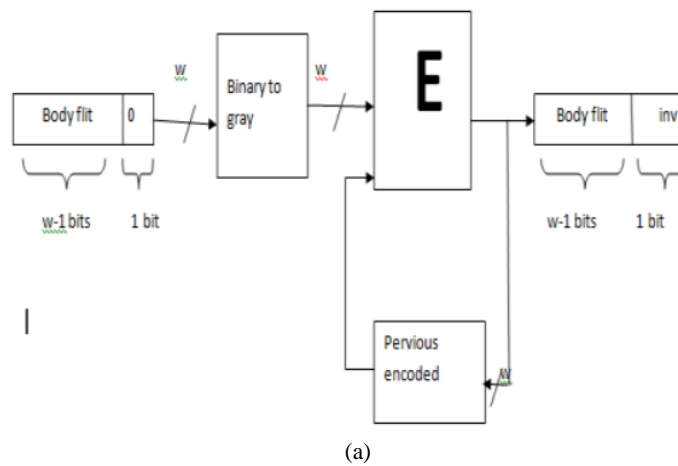


Fig. 1: Scheme-I (a) Block diagram. (b) Architecture of encoder block

$$T_y > T_x \text{ eq..... (2)}$$

$$T_y > 0.5 (w-1) \text{ eq..... (3)}$$

The functional block diagram in Fig.1 show the Scheme-I (a) block diagram (b)) Architecture of encoder block. The w-1 block convert the unique input into encode output. The output of the encoded code is given to input of the encoder block and another input of the encoder block is the before encoded output. The encoder block will compare these 2 input and perform any one of the inversion based on the transition type. The block-E is vary for all 3 scheme. Compare with the present data and earlier encode data to make a decision which inversion is to be performing for link power reduction. Here the ‘TY’ block takes two adjacent bit from the given input. From these two input bits the ‘TY’ block check what type of transition occur, whether more

number of type-1 transition and type-2 transition is happening means it set the output state to '1', or else it set the output to '0'. The odd inversion is performed for these type of transitions. Then the next block is the Majority code it checks the state, if the number of 1's is greater than 0's or not it implement using a simple circuit. The final stage using the XOR circuit, these circuit is used to perform the inversion on odd- bits. The decoding is perform by just invert the encoder circuit when the inverting bit is high.

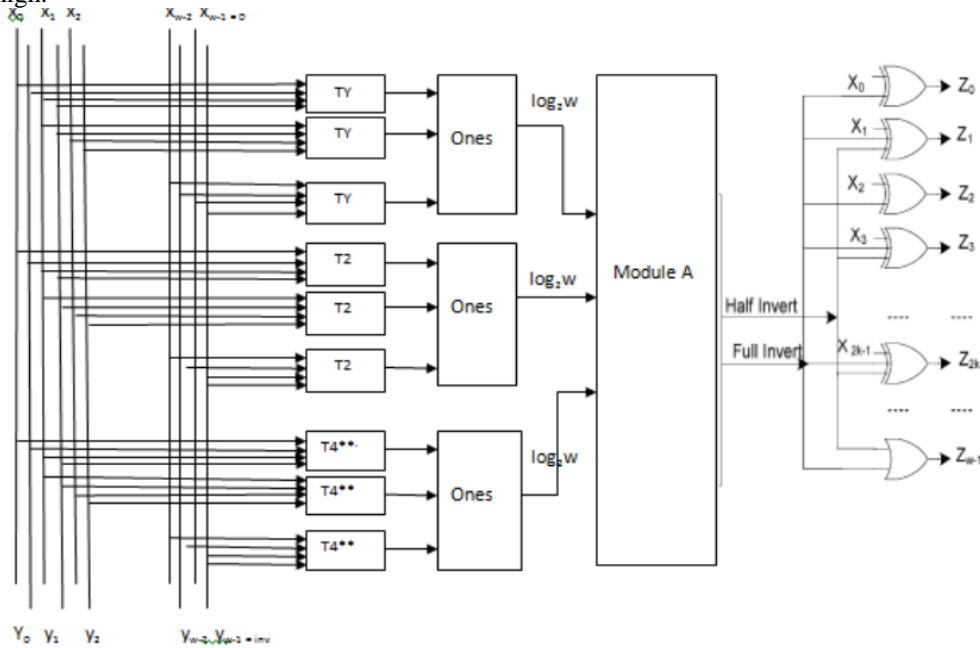


Fig. 2: Encoder architecture scheme-II

B. Scheme II

In the scheme-II encoding, we are going to implement the odd and the full inversion. In these inversion procedure is to convert the Type-II to Type-IV transitions. In these scheme it compare the present data with earlier one it will choose whether we want to do Odd, Full or No inversion to present data which will give power reduction in link.

$$T_2 > T_{4^{**}} \dots\dots\dots (4)$$

Full and odd invert is based on encoding architecture consist of $w-1$ link width and one bit for inversion bit which indicate if the bit travel through the link and it is invert or not. 'W' bits link width is considered when there is no encoding is applied for the input bits. Here the 'Ty' block from scheme-1 is added in scheme-2. This take 2 adjacent bits from the given inputs. From these two input bits the 'Ty' block check what type of transition occur. We have T_2 and $T_{4^{**}}$ blocks which determines if any of the transition types T_2 and $T_{4^{**}}$ occur based on the link power reduction. The number of 1's blocks in the next stage. The output of the T_Y , T_2 and $T_{4^{**}}$ send via number of 1's blocks. The output of the 1's block is $\log_2 w$. The 1st ones block is used to determine the number of transition based on odd inversion. The 2nd ones block determines the number of transition based on the full inversion and the then another one ones block is used to determine the number of transitions based on the full inversion. These inversions are performed based on the link power reduction. Based on these ones block the Module A takes the decision of which inversion should be performed for the link power reduction. For this module is satisfied means the output is set to '1'. None of the output is set to '1' if there is no inversion is takes place. The module A is implement using full adder and comparator circuit.

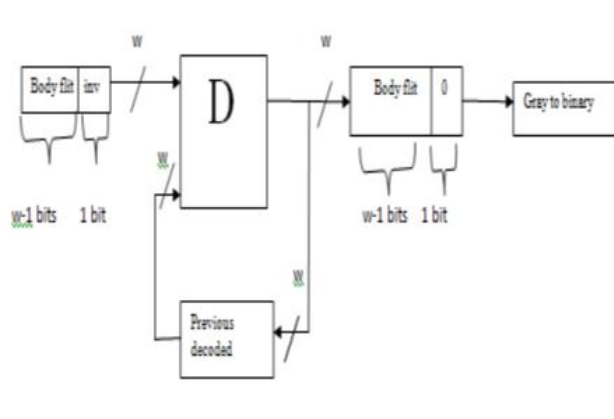


Fig. 3: Block diagram for decoder

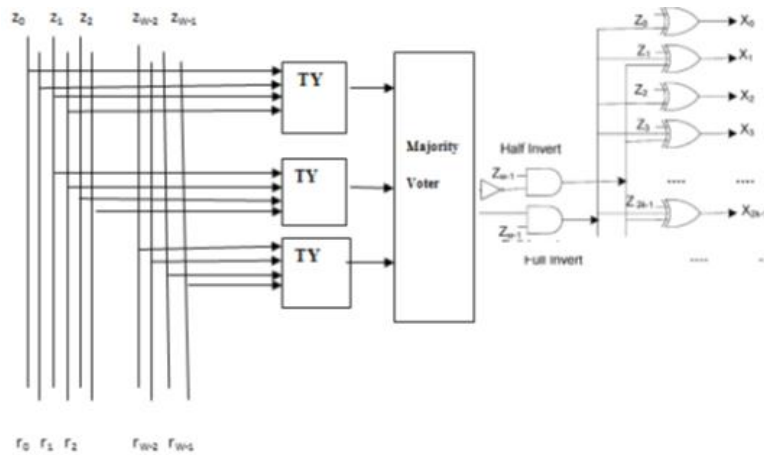


Fig. 4: Decoder architecture scheme-II

The block diagram of the decoder is shown in Fig.3. The $w-1$ bits input is applied in the decoder circuit and another input of the decoder is previous decoded output. The decoder block compare the two input data's and invert operation is performed and $w-1$ bits output is produced. The remaining one bit is used to indicate the inversion is performed or not. Then the decoder output is given to the gray to binary block. This block converts the gray code into original binary input. In decoder circuit diagram (Fig.4.) consist of TY block and Majority vector and XOR circuits. Based on the encoder action the TY block is determined the transitions. Based on the transitions types the majority blocks checks the validity of the inequality given by (2). The output of the majority is given to the XOR circuit. Half inversion, full inversion and no inversion is performed based on the logic gates.

C. Scheme III

In scheme III, we are adding the even inversion into scheme II. Because the odd inversion converts Type-I transitions into Type II transitions. From table II, $T1^{**}/T1^{***}$ are converted into Type IV/Type III transitions by the flits is even inverted. The link power reduction in even inversion is larger than the Odd inversion.

The encoding architecture (Fig.5) in scheme III is same of encoder architecture in scheme I and II . Here we adding the Te block to the scheme II. This is based on even invert condition, Full invert condition and Odd invert condition. It consist of $w-1$ link width input and the w bit is used for the inversion bit. The full, half and even Inversion is performed means the inversion bit is set '1', otherwise it set as '0'. The 'Ty', Te and $T4^{**}$ block determines the transition types $T2$, T_e and $T4^{**}$. The transition types are send to the number of one's block. The Te block is determined if any of the detected transition of types $T2$, $T1^{**}$ and $T1^{**}$. The ones block determines the number of ones in the corresponding transmissions of TY, $T2$, T_e and $T4^{**}$. These numbers of one's is given to the Module-C block. This block check if odd, even, full or no invert action corresponding to the outputs '10', '01', '11' or '00' respectively, should be performed. The decoder architecture of scheme-II and scheme-III are same.

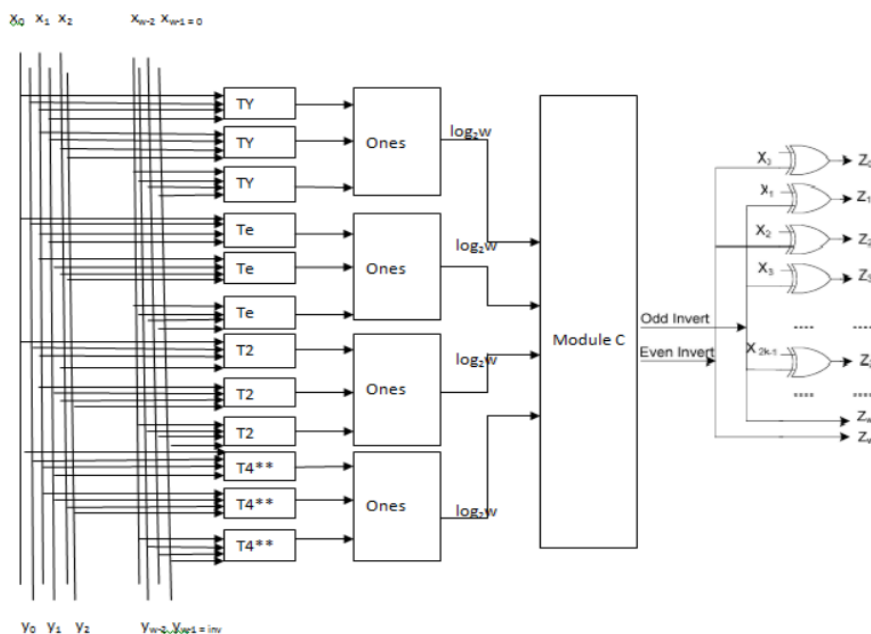
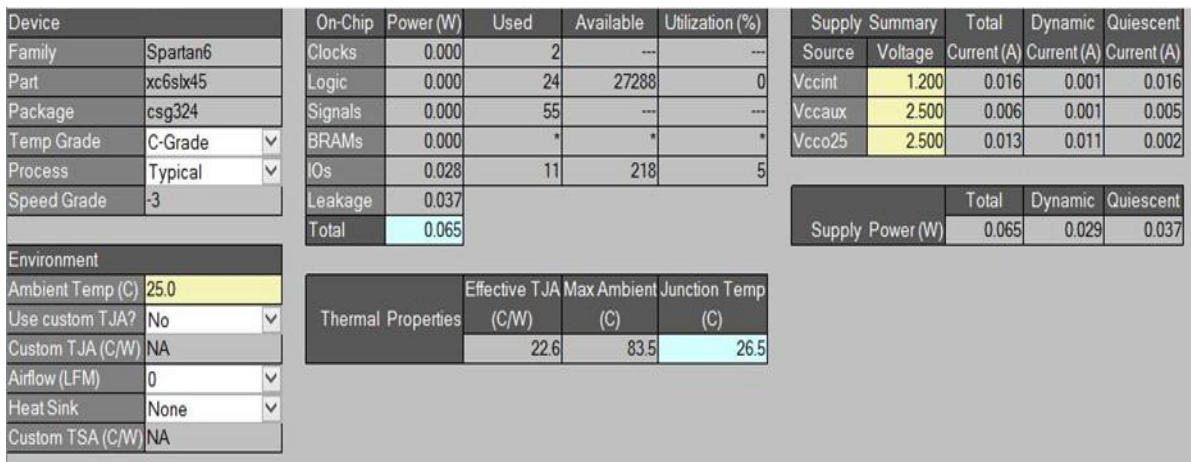
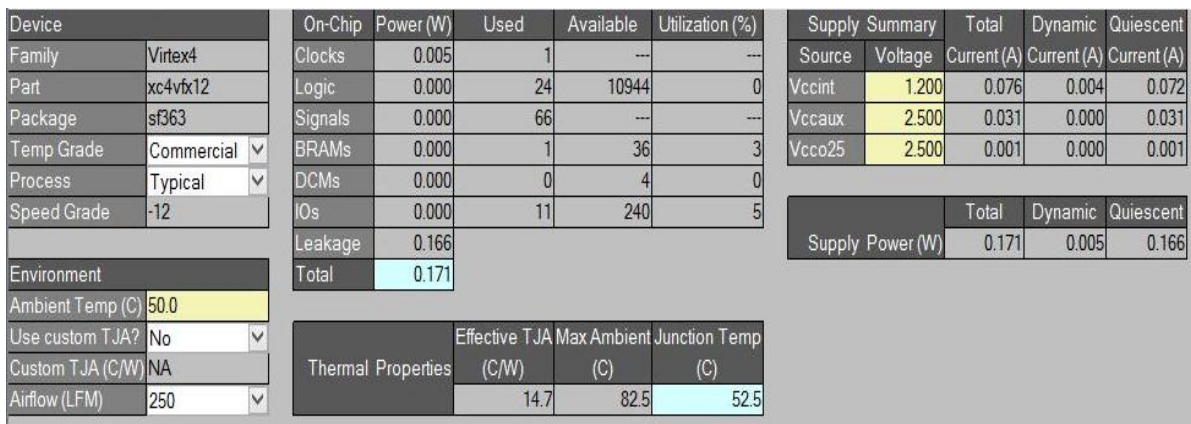


Fig. 5: Encoder architecture for scheme III



(b)
Fig. 7: shows the simulation result of schem-II (a) Output waveform and (b) Power details of Scheme-II



(b)
Fig. 8: shows the simulation result of schem-III (a) Out put waveform and (b) Power details of Scheme-III

VI. CONCLUSION

As compared with the earlier encoding scheme and the proposed technique in the literature, the proposed scheme is minimize not only an switching action, but also the coupling switching action which will be mainly responsible for power dissipation in the link. The proposed encode scheme were agnostic with respect to the fundamental of an NOC architecture in the sense that there applications does not require the any change neither in a router nor in link's. An wide estimation has carry to measure the impact of an encoder and decoder logic's in the NI. The encoder implementation the proposed scheme will be measure in term of the power dissipation and area utilize in the silicon wafer. This impact on the performance, power, and energy metrics has studied

by using a cycle and bit exact NoC simulator under both artificial and real traffic scenario. The application of an proposed encoded scheme which allow saving of energy consumption and power dissipation without any major performance degradation and with less consumption in the NI.

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