

Comparative Analysis of PD and APOD for Cascaded H-Bridge Multilevel Inverter

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Abstract

In recent days multilevel inverter(MLI) hold attractive features, in the area of high power medium voltage energy control though multilevel inverter has a number of advantages it has drawbacks in the vein of higher levels because of using more number of semiconductor switches. So in order to overcome this problem the new multilevel inverter is proposed with reduced number of switches. Switch topologies using carrier-based PWM techniques. These pulse width modulating (PWM) techniques include the phase disposition (PD) strategy, alternate phase opposition disposition (APOD) strategy. The modulating indices are evaluated for total harmonic distortion, form factor, crest factor, VRMS (fundamental) and distortion factor. This paper proposed the different carrier arrangement in order find out the less total harmonics distortion. The results are validated using MATLAB/SIMULINK software.

Keywords: APOD, DF, DPWM, PD, THD

I. MULTILEVEL INVERTER

The term multilevel began with the three level inverter subsequently, several multilevel inverter topologies have been developed. However the elementary concept of multilevel inverter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources can be used as the multiple dc voltage sources. Using multilevel inverter technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved. Among the familiar topologies, the most popular one is cascaded multilevel inverters. It exhibits several attractive features such as simple circuit layout, less components counts, modular in structure and avoid unbalance capacitor voltage problem

There are three main types of transformer less multilevel inverter topologies-the flying capacitor inverter, the diode clamped inverter and the cascaded H-bridge inverter. The flying capacitor inverter is difficult to realize because each capacitor must be charged with different voltages at the voltage level increases. The diode clamped inverter is difficult to expand to multilevel because of the natural problem of the dc link voltage unbalancing. Though the cascaded multilevel inverter requires separate dc sources, it can be expanded An easy way to comply with the conference paper formatting requirements is to use this document as a template and simply type your text into it.

II. OPERATION OF TRINARY DC SOURCES

Fig 1.shows a circuit configuration of a cascaded H-bridge multilevel inverter employing trinary dc input source. It looks like a traditional cascaded H-bridge multilevel inverter except input dc sources. By using V_{dc} and $3V_{dc}$, it can synthesize nine output levels: $-4V_{dc}$, $-3V_{dc}$, $-2V_{dc}$, $-1V_{dc}$, $0V_{dc}$, $2V_{dc}$, $3V_{dc}$,

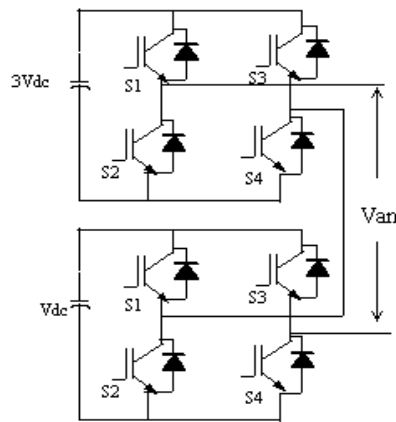


Fig. 1: Configuration of cascaded H-bridge multilevel inverter employing trinary (proposed circuit) Comparison of symmetrical and asymmetrical

Table - 1

| | Symmetrical inverter | Asymmetrical inverter | |
|------------|----------------------|-----------------------|---------|
| | | Binary | Trinary |
| Levels | $2N+1$ | $2^{N+1} - 1$ | 3^N |
| DC sources | N | N | N |
| Switches | $4N$ | $4N$ | $4N$ |

Above comparison shows that the level are increased but switches are reduced.

III. UNIPOLAR SINUSOIDAL PWM METHODS

This work used the intersection of a sine wave with a triangular wave to generate firing pulses for a nine level inverter. There are many alternative strategies to implement this. They are as given below.

- 1) Phase disposition PWM strategy.
- 2) Alternate phase opposition disposition PWM strategy.

A. Phase Disposition PWM Strategy

For an m-level inverter, $(m-1)/2$ triangular carriers of the same frequency f_c and the same peak to-peak amplitude A_c are disposed so that the bands they occupy are contiguous. The carrier set is placed above the zero reference.

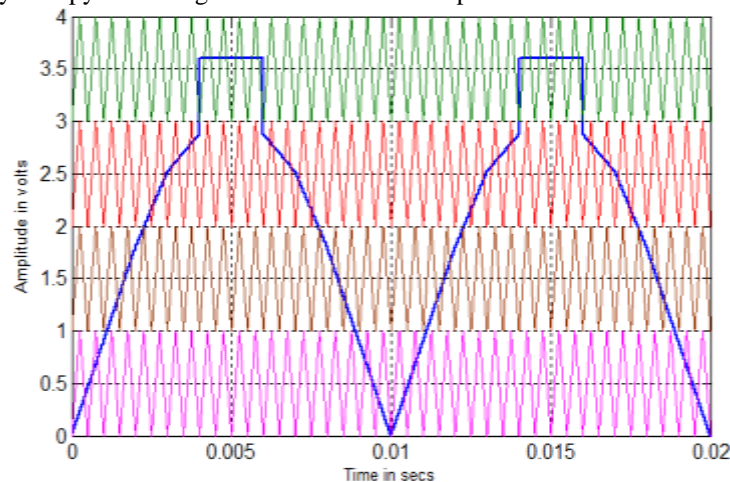


Fig. 2: Carrier arrangements for PDPWM strategy ($m_a = 0.9$ and $m_f=40$)

B. Alternate Phase Opposition Disposition PWM Strategy. Carriers Are Arranged In Such A Manner That Each Carrier Is Out Of Phase With Its Neighbour By 180 Degrees.

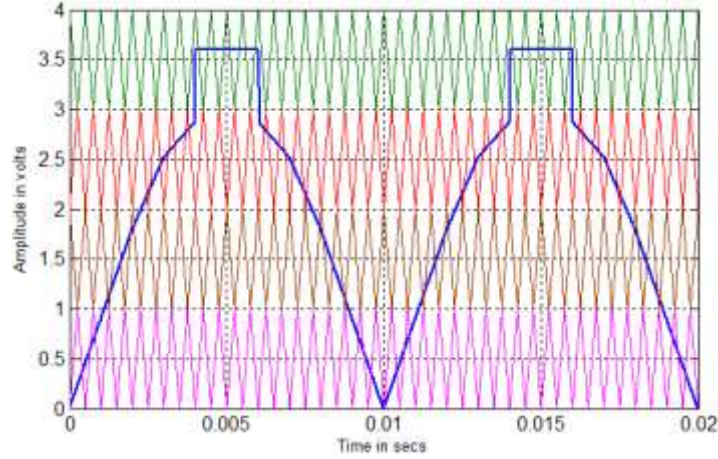


Fig. 3: Carrier arrangements for APODPWM strategy ($m_a = 0.9$ and $m_f = 40$)

IV. SIMULATION RESULT

At first, we are performed computer-aided simulations to prove availability of the proposed multilevel inverter. And it was considered to a pure resistive load. If paragraphs must be indented.

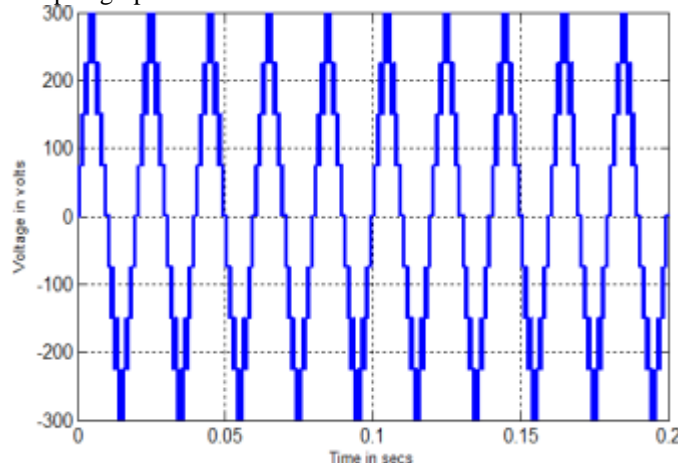


Fig. 4: Carrier arrangement for PDPWM strategy ($m_a = 0.9$ and $m_f = 40$)

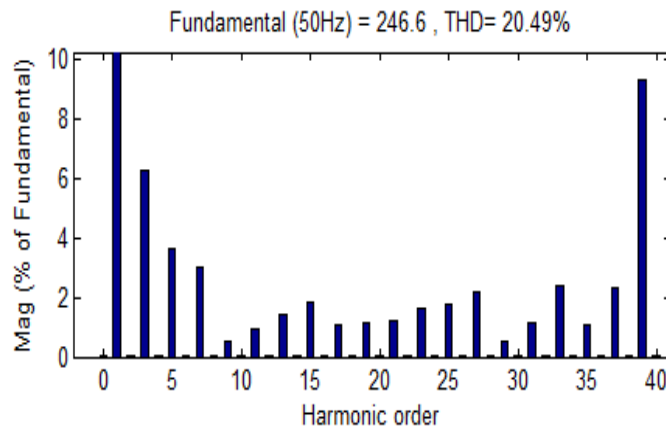


Fig. 5: FFT-harmonic spectrum of output of PDPWM strategy

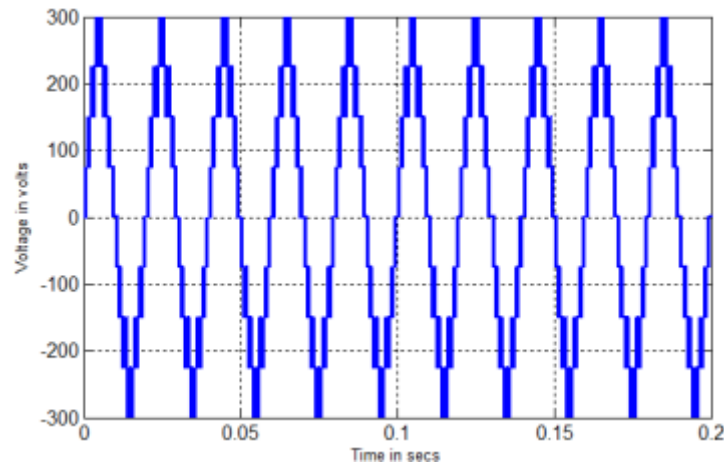


Fig. 6: Carrier arrangement for APODPWM strategy ($m_a=0.9$ and $m_f=40$)

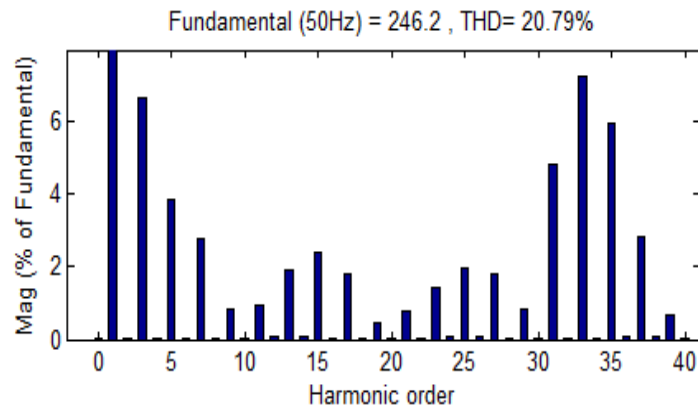


Fig. 7: FFT-harmonic spectrum of output of APODPWM strategy

Multilevel inverter is modelled in SIMULINK using power system block set. Simulations are performed for five different values of modulation indices and the corresponding %THD are measured using the FFT block and their values are shown in table V and figs. 4-7 shows the simulated output voltages of asymmetric reduced switch multilevel inverter and their harmonic spectrum with above strategies but for only one sample value of $m_a=0.9$. Fig.4 shows that the 9 level output voltage generated by PDPWM strategy and its FFT plot is shown in Fig.7. Fig.6 shows the 9 level output voltage generated by APOD strategy and its FFT plot.

Table - 2
VRMS for modulation Indices with sinusoidal references

| M_a | APOD | PD |
|-------|-------|-------|
| 1 | 193.2 | 192.6 |
| 0.95 | 183.4 | 183.4 |
| 0.9 | 174.1 | 174.4 |
| 0.85 | 164.4 | 164.2 |
| 0.8 | 154.6 | 154.7 |

Table - 3
Crest Factor for modulation Indices with sinusoidal references

| m_a | APOD | PD |
|-------|---------|---------|
| 1 | 1.41407 | 1.41433 |
| 0.95 | 1.41384 | 1.41384 |
| 0.9 | 1.41412 | 1.41399 |
| 0.85 | 1.41362 | 1.41473 |
| 0.8 | 1.41461 | 1.41435 |

Table – 4
Form Factor for modulation Indices with sinusoidal references

| <i>ma</i> | <i>APOD</i> | <i>PD</i> |
|-----------|-------------|-----------|
| 1 | 1.56E+05 | 5.13E+03 |
| 0.95 | 4.10E+04 | 5.95E+04 |
| 0.9 | 2.32E+03 | 4.65E+03 |
| 0.85 | 2.19E+03 | 2.18E+03 |
| 0.8 | 4.12E+03 | 4.12E+03 |

Table - 5
THD for modulation Indices with sinusoidal references

| <i>ma</i> | <i>APOD</i> | <i>PD</i> |
|-----------|-------------|-----------|
| 1 | 16.21% | 16.37% |
| 0.95 | 18.80% | 18.61% |
| 0.9 | 20.79% | 20.49% |
| 0.85 | 21.67% | 21.87% |
| 0.8 | 21.77% | 22.03% |

V. CONCLUSION

In this paper various PWM strategies are used and have been developed using MATLAB SIMULINK model and analyzed for different modulation indices ranging from 1-0.8. Various performance factor like T.H.D, C.F which is a measure of the stress on the devices, VRMS indicating the amount of DC bus utilization have been evaluated presented and analyzed. The T.H.D is low in PD strategies as compared with APOD method at 0.9 modulation index and the proposed a cascaded H-bridge multilevel inverter employing trinary dc sources to obtain a large number of output voltage levels with minimum devices. The proposed inverter can synthesize high quality output voltage near to sinusoidal waves. The circuit configuration is simple and easy to control.

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