

Design of CMOS Based Numerical Control Oscillator with Better Performance Parameter in 45nm CMOS Process

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Abstract

Numerically Controlled Oscillator (NCO) is an important component in many Digital Communication Systems such as Digital Radio and Modems, Software Defined Radios, Digital Down/Up converters for Cellular and PCS base stations etc. This work presents a technique for the generation of analog sinusoidal signals with high spectra quality and reduced circuitry resources. A common method for digitally Generating a complex or real valued sinusoid employs a Look-Up table based scheme. NCO is a new technology of Frequency synthesis; It is developed the using third generation of Frequency synthesis technology. The technique of NCO is gaining popularity as a method of generating Sinusoidal signals and modulated signals in digital systems. The test Results are matching with theoretical and simulated results. Numerically Controlled Oscillator (NCO) is an important component in many Digital Communication Systems such as Digital Radio and Modems, Software Defined Radios, Digital Down/Up converters for Cellular and PCS base stations etc. The NCO Design is first simulated and optimized on the software tool MICROWIND 3.5 using a standard 45 nm technology.

Keywords: Numerically Controlled Oscillator, CMOS, PA, PAC, Look Up Table

I. INTRODUCTION

A key requirement in most applications is the ability to generate & control waveforms at various frequencies. Advantages of Numerically Controlled Oscillators over other types of oscillators in terms of agility, accuracy, stability & reliability. Numerically Controlled Oscillator (NCO) is an important component in many Digital Communication Systems such as Digital Radio and Modems, Software Defined Radios, Digital Down/Up converters for Cellular and PCS base stations, etc. The technique of NCO is gaining popularity as a method of generating sinusoidal signals and modulated signals in digital systems.

This paper is organized as follows, in section II, the basic architecture of ROM-based NCO is described and the main challenges of NCO design are discussed. In section III, the NCO Architecture is presented. Physical design, implementation and simulation results done using Microwind Software tool along with the optimization. Finally; section IV concludes this paper with Summary.

II. NCO OVERVIEW

A. Architecture of NCO:

NCO is a digital signal generator which creates a synchronous discrete-time, discrete-valued representation of a waveform, usually sinusoidal. Figure 1 shows the block diagram of a NCO system. The NCO produces sinusoidal signals at a given frequency setting word (FSW) which determines the phase step. Once set, this digital word determines the sine wave frequency to be produced. The phase accumulator output than continuously produces proper binary words indicating the instantaneous phase to the table look-up function.

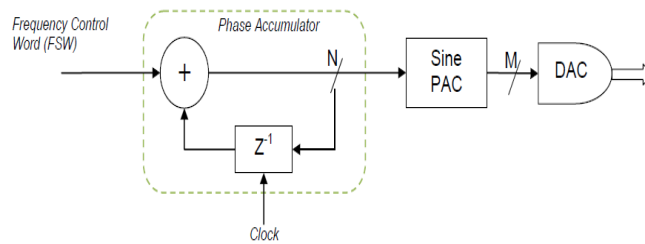


Fig. 1: Block Diagram of a NCO system

The digital part of the NCO consists of the phase accumulator and the LUT. The frequency of the output signal for signal N-bit system is determined by following equation,

$$f_{out} = \frac{K \times f_{clk}}{2^N}$$

Where, K - frequency setting word (FSW), Fclk- system clock frequency and N- number of bits that the phase accumulator can handle.

NCO generally consists of three parts:-

- A. Phase Accumulator (PA)
- B. Phase to Amplitude converter (PAC)
- C. Digital to analog converter (DAC)

B. Phase accumulator (PA):

A binary phase accumulator consists of an N-bit binary adder and a register configured as shown in figure below. Each clock cycle produces a new N-bit output consisting of the previous output obtained from the register summed with the frequency control word (FCW) which is constant for a given output frequency. The resulting output waveform is a staircase with step size F, the integer value of the FCW. In some configurations, the phase output is taken from the output of the register which introduces one clock cycle latency but allows the adder to operate at a higher clock rate.

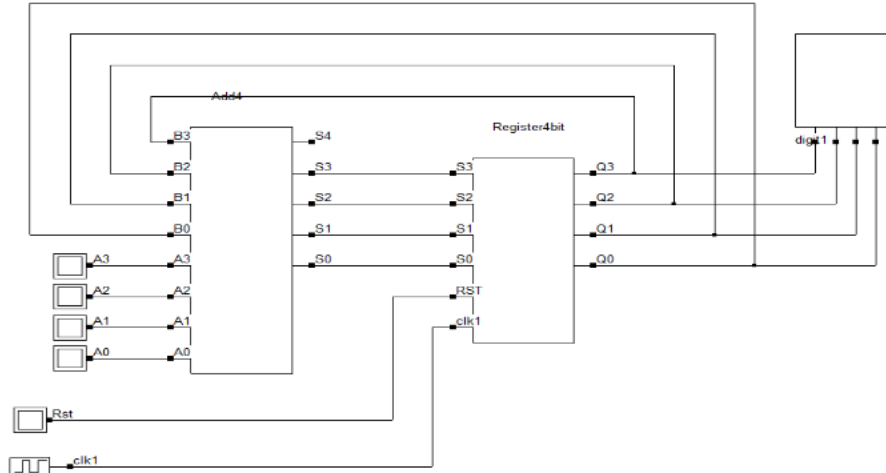


Fig. 2: Top level entity of an accumulator

Above schematic is for top level entity of an accumulator, which itself is made of two modules a 4 bit adder and 4 bit register. We have considered only 4 bits off adder as our PAC is of 4 bits. The bits A0 through A3 are frequency select words which are used to control op frequency of an NCO. FSW controls the step size of a counter .By setting its value by one we allow counter to run from 0 to 15. The role of an accumulator module is to generate address locations for PAC to fetch a sine value from LUT.

C. Phase to Amplitude Converter (PAC):

The phase-amplitude converter creates the sample-domain waveform from the truncated phase output word received from the PA. The PAC can be a simple read only memory containing 2M contiguous samples of the desired output waveform which typically is a sinusoid. Oftentimes though, various tricks are employed to reduce the amount of memory required. This includes various trigonometric expansions, trigonometric approximations and methods which take advantage of the quadrature symmetry exhibited by sinusoids. Alternately, the PAC may consist of random access memory which can be filled as desired to create an arbitrary waveform generator. It uses the phase accumulator output. Phase accumulator output word (phase word) as an index

into a waveform look-up table to provide a corresponding amplitude sample. If the PAC capacity is 2 M, the PA output word must be truncated to M bits.

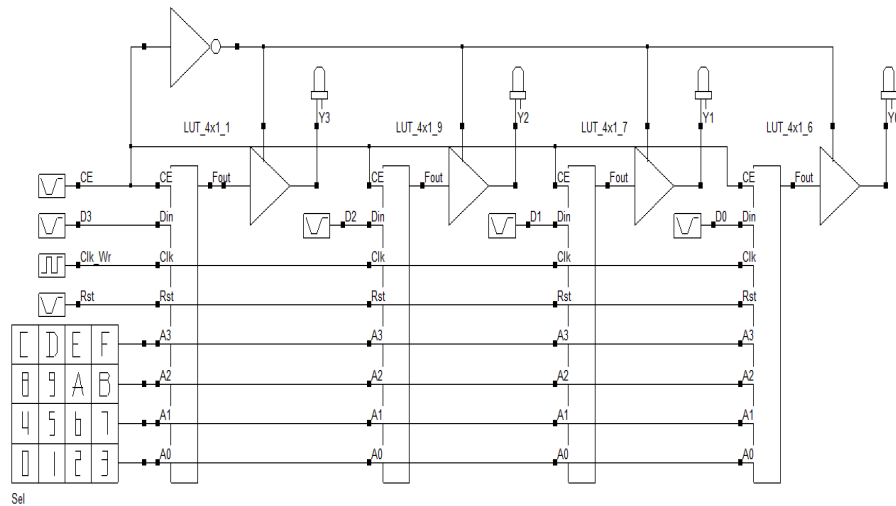


Fig. 3: PAC Realization

D. Digital to Analog Converter (DAC):

Here we use R-2R design based digital to analog converter. It consists of a network of resistors alternating between R and 2R. For an N bits DAC, only N cells based on 2 resistors R and 2R in series are required. It is not easy to construct a resistor-based DAC with a high resolution, due to the resistance spread and to the needs for 2N serial resistors.

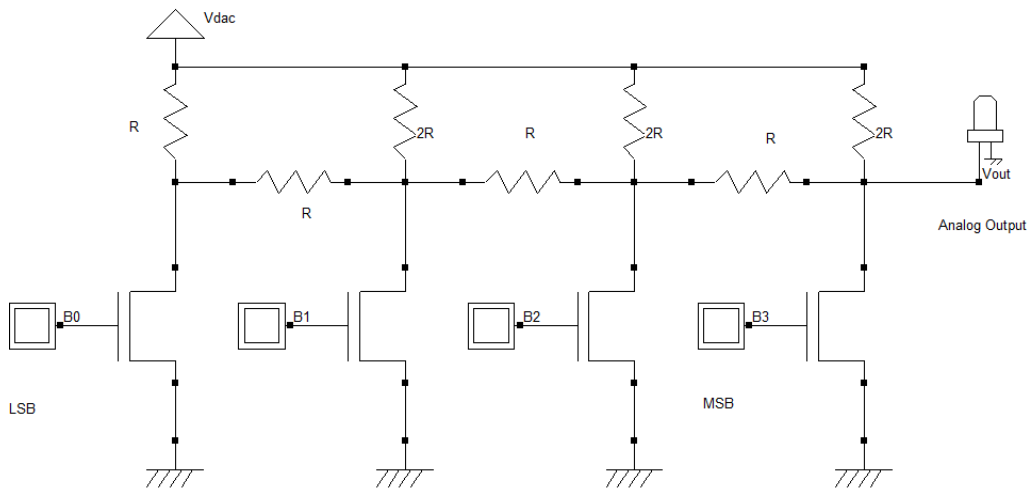


Fig. 4: Physical design of 4 bit R2R DAC

We used Seven resistors were used for the 4-bit implementation of the R-2R DAC, that is half of the simple R-ladder. The difference is even more significant in the 8-bit circuit, with only 15 resistors, while the simple ladder would require 255 resistors in series. In the 8-bit implementation of the DAC, the digital inputs (B7..... B0) determine whether each cell is switched to ground or tied to Vdac. Each cell's output voltage is a ratio of Vdac because of the ladder network voltage division. The final output voltage VOUT depends on the value of B (0 to 15), following the given formula:

$$Vout = Vdac \cdot \frac{(2^N - B)}{2^N}$$

The simulation of the four bit 2-2R digital to analog converter shows a regular decrease of the output voltage Vout.

E. NCO Implementation:

Now we are having all required three blocks that we need for the designing of the NCO. Here we are going to arrange all these three for realization of the NCO.

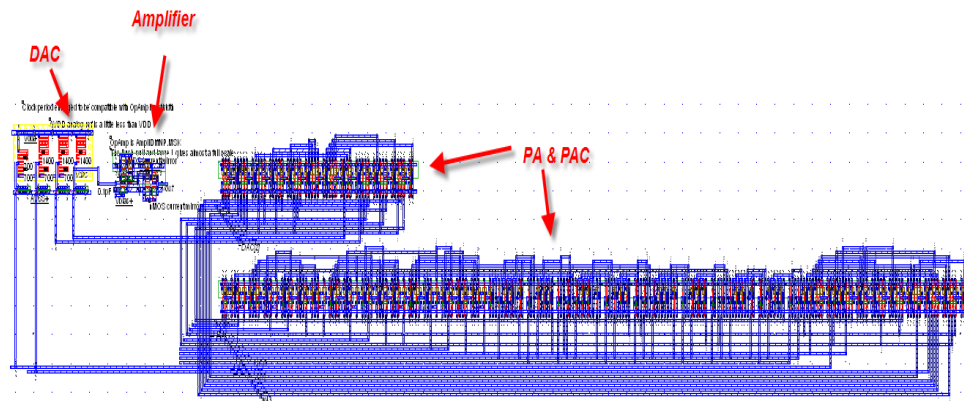


Fig. 5: Physical Layout design of NCO

Digital to Analog Converter (DAC) is added at the outputs (DAC) coming from PAC. This DAC is made up using R-2R resistive ladder network. To improve the DAC range and level, a push-pull amplifier is added at DAC output, which is a differential amplifier.

F. Physical Design Parameters:

Width: 85.1µm (4257 lambda)
 Height: 57.4µm (2868 lambda)
 Surf: 4883.6µm² (0.0 mm²)

G. Simulation Results:

For simulation here are the details

Rst = A pulse applied at start up.

Clk_NCO = 500 MHZ clock (1ns low & 1 ns high)

A0 = Clock applied which is high for first 100 ns, then low for next 100 ns

A1 = Clock applied which is low for first 100 ns, then high for next 100 ns, would give a 2 range of FSW, 1 & 2, more can be applied by changing them.

Vdac = DAC output, Vout = amplifier output, FSW = 1 and N = 4.

For calculating Frequency Resolution, we are having formula as;

$$F_{res} = \frac{Clk_{NCO}}{2^N}$$

By putting these values in the equation;

Fres = 500MHz/16= 31.25 MHz

Where, FSW = Frequency select word

Fout = FSW x Fres

For FSW = 1 Fout = 1 x 31.25 Mhz = 31.25 MHz

For FSW = 2 Fout = 2 x 31.25 Mhz = 62.5 MHz

III. CONCLUSION

This paper presents the simulation and Implementation of NCO. The Design and Realization of NCO include sub modules like phase Accumulator, Phase to amplitude Converter for Look-Up Table and Digital to analog converter for creating a sinusoidal waveform. Design, Area and power parameters are optimized by working on physical layout design. There are plenty of applications of a sine wave, because it forms the basic function for most of the electrical and electronic systems. Using the Numerically Controlled Oscillator (NCO) module to generate a sine wave at any desired frequency. Here we have implemented 4 bit NCO structure, with two ranges of frequencies. From this results could conclude that conversion is performed for all combination successfully and a low-power 4-bit NCO in a 45 nm CMOS process with a 1 V supply voltage is designed.

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REFERENCES

- [1] Etienne Sicard, Chen Xi, A Pc- Based Educational Tool For Cmos Integrated Circuit Design, Insa, Department Of Electrical & Computer Engineering Av De Ranguel
- [2] Cmos Integrated Analog To Digital & Digital To Analog Converters, 2nd Ed., Rudy Van Deplasseche
- [3] Numerically Controlled Oscillator, Lattice Semiconductor Corporation, 2009
- [4] Gopal D. Ghiwala, Pinakin P. Thaker, Gireeja D. Amin, Sr. Scientist/ Engg. Satd, Sac (Isro), Ahmedabad L.C. Institute Of Technology, Bhandu "Realization Of Fpga Based Numerically Controlled Oscillator" Iosr Journal Of Vlsi And Signal Processing, 2013
- [5] P.O. Bishop, Neurophysiology Of Binocular Vision In J. Houseman [Ed], Handbook Of Physiology, 4 (New York; Springer- Verlag, 1970) 342-36.
- [6] Jane Radatz, The Ieee Standard Dictionary Of Electrical & Electronics Terms, Ieee Standards Office, New York, Ny, 1997.