Implementation of Physical Design of Ternary Inverter with Improved Characteristic

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Abstract

The ternary logic (also called three-valued or trivalent logic and abbreviated 3VL) is a promising alternative to the conventional binary logic design technique. It is possible for ternary logic to achieve simplicity and energy efficiency in digital design since the logic reduces the complexity of interconnects and chip area, in turn reducing the chip delay. It offers better utilization of transmission channels because of the higher information content carried by each line, also gives more efficient error detection and correction codes and possess potentially higher density of information storage. The proposed paper is aimed to achieve the low power consumption, high stability physical design of ternary inverter. Here we used Microwind EDA tool for designing and simulation of the physical design.

Keywords: MVL, Ternary arithmetic, CMOS 45 nm Technology, Physical Design

I. INTRODUCTION

With the fast advancement of CMOS technology, more & more signal processing functions are implemented in the digital domain for low cost, low power consumption, higher yield, & higher re - configurability. The more and functions discrete components requires the larger memory size for restoring the logic for specific applications. The binary arithmetic provided you a better solution for the memory implementation but required more number of lines to store and retrieve the data.

The main solution for the implementation is a Multi valued logic design systems. The chip area and power dissipation of MVL multiplier implementation reduced to half that of the fastest conventional binary realization of the same multiplier. In modern CMOS technology, another important part of the power consumption is due to the global clock needed to synchronize the system, because of its long switching activity behavior.

In theoretical aspect, multivalued circuits have many advantages over their binary circuits

1) In MVL, each wire can transmit more information than binary, the number of connections inside the chip can be reduced.
2) MVL element can process more information than a binary element, the complexity of circuits may be decreased
3) The on- and off-chip connections can be reduced to help the pin-out difficulties that arise with increasingly larger chips
4) The speed of serial information transmission is faster since the transmitted information time is increased.

Also practical implementations of Multi valued logic arithmetic will provides advantages which are very wide and very feasible for number representation, processors designing, communication network, electronics converters and Memory designing.

In number system, for representing decimal number 16 in binary, 5 bits are required (10000) whereas for representing same number in ternary require 3 bits (121). Similarly, signed number representation in binary ranges from -2 n-1 to 2 n-1 -1 for negative & positive numbers. In ternary same range spans from -3n-1 to 3n-1 -1. Thus number representation in ternary facilities to develop algorithm for arithmetic operations for high speed and/or area efficient computation.

Likewise the same in Memory designing number of bits required to code a decimal number in binary is more than ternary, ultimately memory required to store the coded decimal in ternary is lesser than binary which has advantages like cost/bit ratio reduction, reduced access time & increased storage capacity

II. TERNARY SWITCHING ALGEBRA

Ternary has the logic levels „0" corresponding to logic-0 in binary (also called zero element or low voltage), "1" corresponding to an intermediate stage (also called Meta stable state) and "2" corresponds to logic-1 in binary (also called universal element or high voltage). The intermediate state can be metaphorically thought of as either true or false. The binary logic is limited to only two states "1" and "0", whereas MVL is a set of finite or infinite number of values. In a standard CMOS process, the three supply voltages are vdd, vdd/2 and ground. Ternary logic gates are the basic building blocks in realizing combinational and

sequential logic functions. The implementation is based around (bipolar transistors, MOSFETs etc.) a basic switching elements, which is referred to as T-Gates.

The Ternary gate called T-gate qualifies as a universal element in several different senses. Firstly, it should be logically complete with simple operation. Secondly, it should be easily implemented with its straightforward construction. Thirdly, it should possess two essential elements that must be embodied in any logic gate, namely, logic-value thresholding and logic-signal connection of switching. This functional completeness of T-gate is the property of a set of compositions which enables one to synthesize any arbitrary switching function within a particular class. There are several algebras available for the design of ternary switching functions among which, the Post and the Modular algebra h have the advantages of similarity with ordinary algebra.

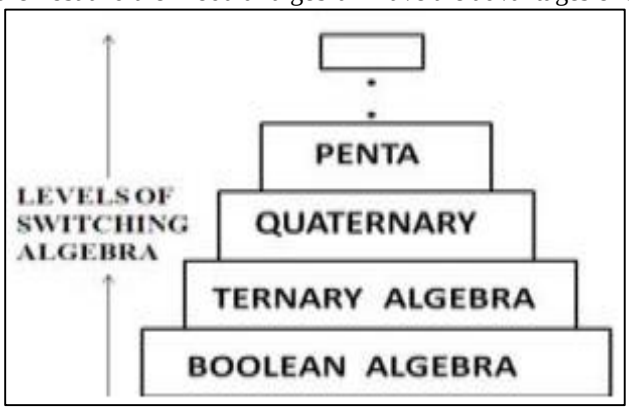

Fig. 1: Levels of switching algebra

THREE-VALUED, or ternary, logic offers several important advantages over binary logic in the design of digital systems. For example, more information can be transmitted over a given set of lines or stored for a given register length, the complexity of interconnections can be reduced, reduction in chip area can be achieved, and more efficient error-detection and error-correction codes can be employed. Furthermore, serial and some serial-parallel arithmetic operations can be carried out at higher speeds. Most of these advantages have a direct bearing on the VLSI implementation of digital systems, and as a result several realizations of basic ternary gates have been proposed in the literature. These have been shown to be useful for the design of "ternary computers," for digital filtering, and for various other applications.

III. PROPOSED 6 TRANSISTOR TERNARY INVERTER

A general ternary inverter (GTI) is a basic unary operator with one input x and three outputs. Therefore, the implementation of ternary inverter requires three inverters namely negative ternary inverter (NTI), standard or simple ternary inverter (STI) and positive ternary inverter (PTI) forming an operator set that is complete in logic sense.

Table – 1
Truth table of T-Inverter

Input	*Output*
0	*2*
1	*1*
2	*0*

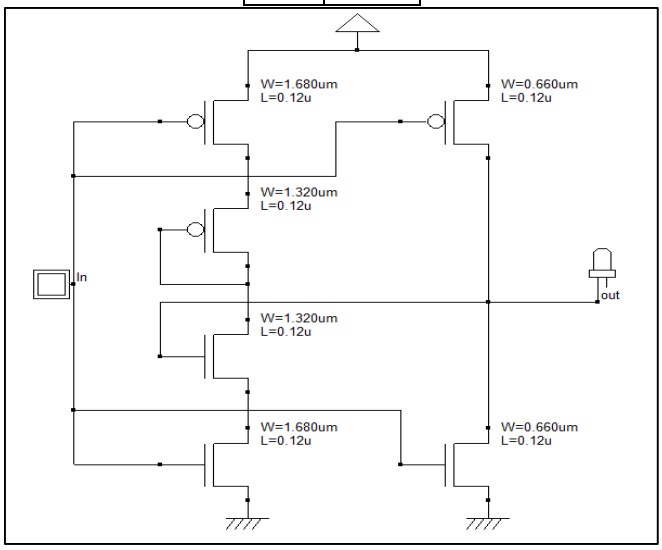

Fig. 2: Proposed Schematic Design of GTI

Six transistor ternary inverter is shown in figure 2. Here the main operation is depends upon various factors of transistor. The threshold voltages of T1, T2, and T3 are 0.392, 0.387, and 0.398 V, respectively The threshold voltages of T5, T6, and T4 are 0.460, 0.459, and 0.464 V, respectively.

When the input voltage changes from low to high at the power supply voltage of 1.2 V, initially, the input voltage is lower than 300 mV. This makes both T5 and T6 turn ON, both T1 and T2 turn OFF, and the output voltage becomes 1.2V, i.e. logic 2. As the input voltage increases beyond 300 mV, T6 is OFF and T5 is still ON. Meanwhile, T1 is ON and T2 is OFF. The diode connected CNTFETs T4 and T3 produce a voltage drop of 0.45 V from node n2 to the output, and from the output to n1 due to the threshold voltages of T4 and T3.

Therefore, the output voltage becomes 0.6 V, i.e., half of the power supply voltage.

As we know that, half Vdd (Vdd/2=0.6 V) represents logic 1. Once the input voltage exceeds 0.6 V, both T5 and T6 are OFF, and T2 is ON to pull the output voltage down to zero. The input voltage transition from high to low transition is similar to the low to high transition.

For obtaining the threshold voltages prescribed above, we have to adjust the Width and Length ration in such a manner that the transistor can provides the switching in accordance with the current.

Here, we designed six transistor ternary inverter with improved noise margin. For this, we select the Width as,

Table – 2
Width and Length for NMOS and PMOS Transistor

Transistor	*Width (W)*	*Length (L)*	*Current (I)*	*Threshold Vtg (Vth)*
T1	*1.680um*	*0.120um*	*3.400mA*	*0.392V*
T2	*0.660um*	*0.120um*	*1.336mA*	*0.387V*
T3	*1.320um*	*0.120um*	*2.672mA*	*0.398V*
T4	*1.320um*	*0.120um*	*1.101mA*	*0.392V*
T5	*1.680um*	*0.120um*	*1.401mA*	*0.460V*
T6	*0.660um*	*0.120um*	*0.550mA*	*0.550V*

IV. PHYSICAL LAYOUT DESIGN

Now we are having the width and length values for each transistor that we are planning to design. Generate the transistor putting the values and placed the component on the substrate.

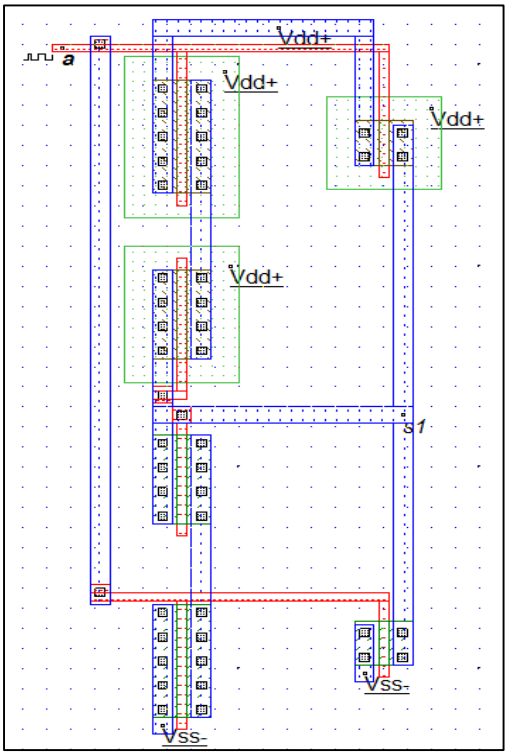

Fig. 3: Physical design of Ternary Inverter

Physical Parameters
Width: 1.6µm (81 lambda)
Height: 3.5µm (177 lambda)
Surf: 5.7µm2 (0.0 mm2)

For simulation of the ternary arithmetic circuits, we need to design a special type of input which will exhibit three voltage levels. In microwind software tool, we can use several number on input forms. The input form PWL stands for Piese-wise-linear. In such form of input, we can provide the sequence of input in the data stream format. It is the special type of input which is useful for worst case delay finding in any combinational circuits. It provides you two voltage levels as shown in figure as level 0 and level 1. For 45 nm CMOS technology, the Vdd is 1 V, as level 1 and we start the input value from 0, as level 0. In this case, our input will start from 0v and will ends up at 1v.

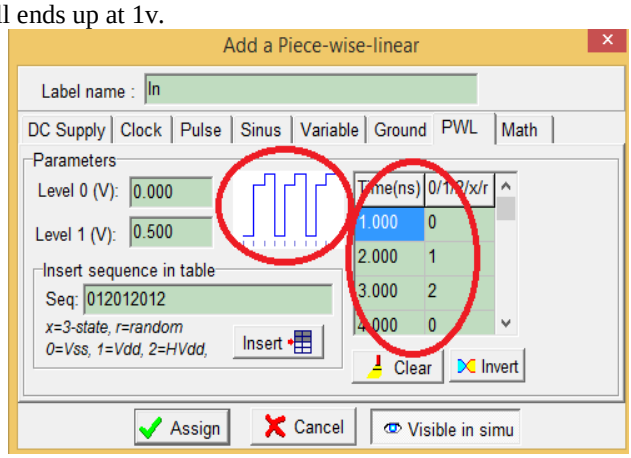

Fig. 4: Three level input form with voltage levels

After assigning the PWL to the physical design, the simulation shown n figure 5.

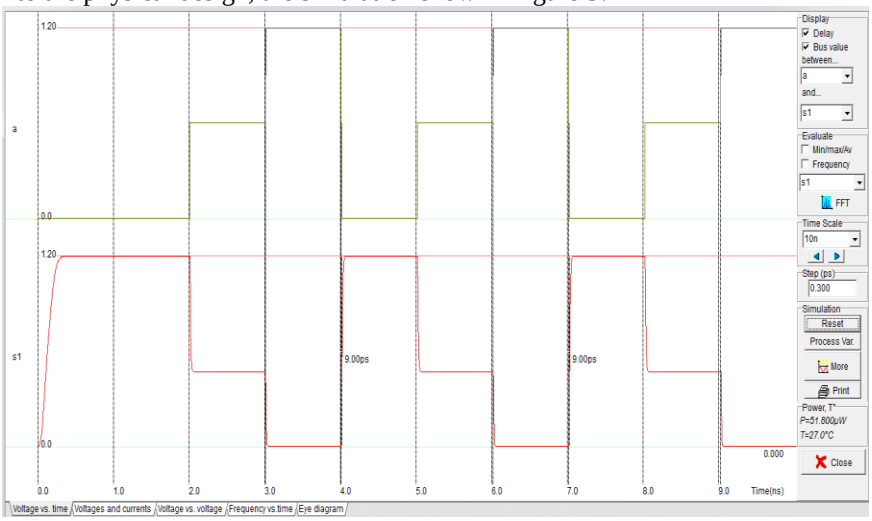

Fig. 5: Transient analysis for voltage

The above simulated output shows the transient analysis of voltage. As per the truth table we are coming across the values of output.

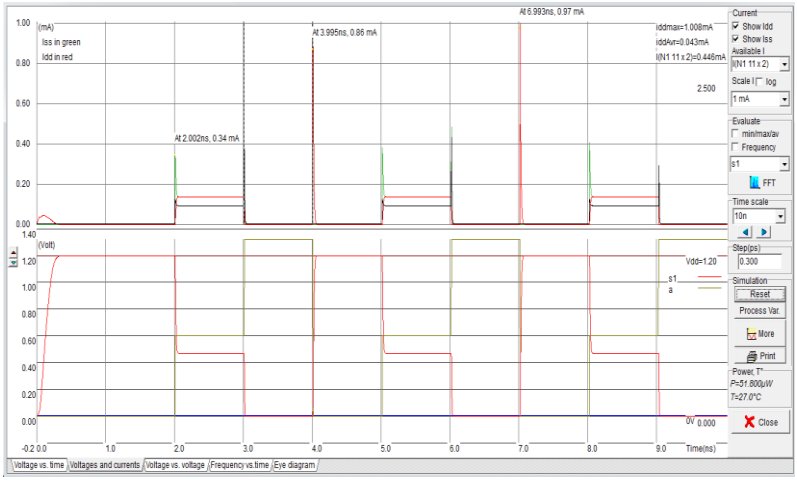

Fig. 6: Transient analysis for Current

From the above simulated output, the maximum current; Iddmax is 0.347mA and the average current of the design, IddAvr is 0.023mA. So as per the application we can design the T-inverter by again setting the values of Width and Length of the transistors.

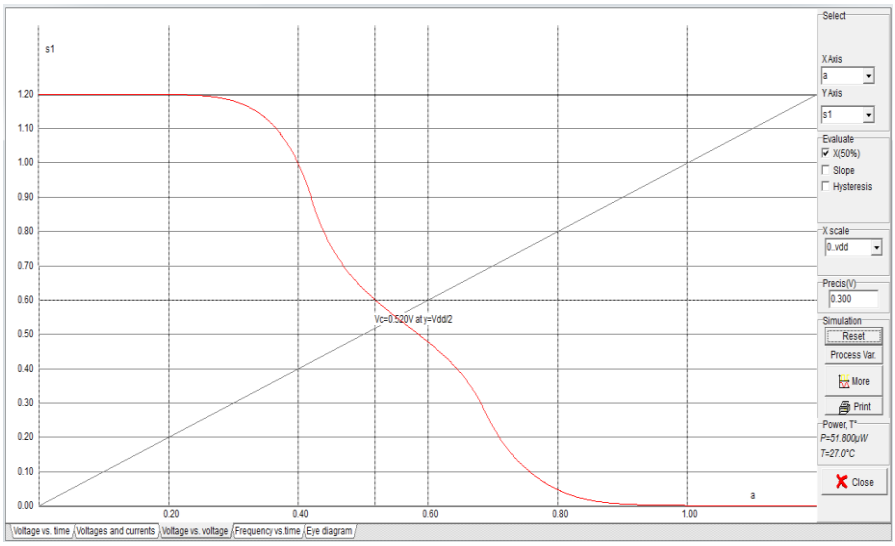

Fig. 7: DC Transfer characteristic

The DC/Voltage transfer characteristics of the STI in Figure. Compared with the conventional STI design in Fig.3, the proposed STI design provides a larger noise margin, which is a positive feature for low power supply circuits. Furthermore, the proposed STI achieves a rail to rail output swing in contrast to the STI design shown in Fig.7.

Eye diagram is nothing but the continuous overlapping of the rise time and the fall time. It will provide you the direct values of noise margin and propagation delays.

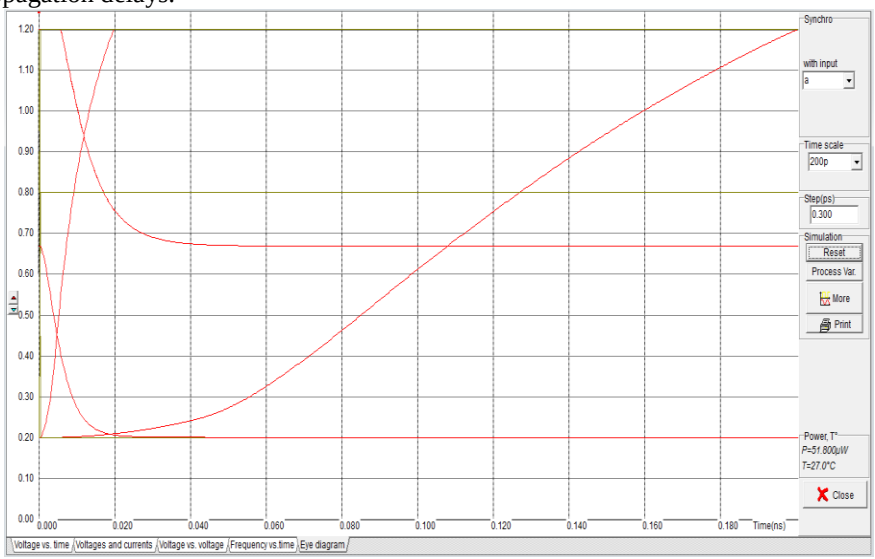

Fig. 8: Eye Diagram

V. CONCLUSION

This paper presents the simulation and Implementation of and simulation of CMOS based circuitry. Here for the design, Microwind 3.5 VLSI Backend software is used for generating, designing and testing ternary circuits. This software allows designing and simulating an integrated circuit at physical description level.

The operating point which is called as commutation pint plays a vital role which we can find out from DC transfer characteristics of the CMOS circuit. Ideally the commutation pint should half of the VDD. For our design, the VDD is 1 V and for a perfect designed, it must be 0.5. For our physical design simulation we are coming across 0.520 as commutation value which is very fine with physical implementation.

Also the on screen current estimation is Iddmax is 0.347mA and IddAvr is 0.023mA, which is very low with CMOS 45 nm technology. The design uses 51.600uW as power consumption.

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