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Valley-Fill Circuit for Power Quality Improvement

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Abstract

Power factor is an important performance parameter of electric network. This parameter becomes very significant when power electronics circuits are used in different application. Active power factor is one of the method used to improve the power factor but it is very costly. Valley fill circuit is a passive power factor used with power electronic circuit particularly with artificial light application. The objective of this paper is to analyze valley fill circuit with simulation and hardware. Simulation is done by using PSIM simulation software and a prototype hardware is made for comparison
Keywords: Power factor, Valley Fill, Power Electronics, PSIM, Power quality

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I. INTRODUCTION

Power factor is an important power quality performance parameter for electrical network. Applications where power electronic circuits are used always faces the danger of poor power quality [1]. Electronic control system [ECS] for artificial lighting is one of the power electronic application [2-3]. Various types of electronic control systems are developed for artificial light sources [4-8]. In some of the ECS active power factor correction technique is used to improve the power factor on AC side [9-11]. The active power factor correction is very effective but very costly. Consumers of developing countries like India needs a low cost solution. Valley fill is a passive power factor correction circuit used extensively in ECS for lighting applications [12-13]. The main aim of this paper is to analyze the working of valley fill circuit. A simulation study is done using PSIM simulation software and hardware prototype is made for comparison with simulation results. The results are compared with and without Valley Fill Circuit and significant improvement is seen in power factor.

II. VALLEY FILL CIRCUIT

The circuit functioning can be summarized as follows, the rectified current charges the capacitor and flows to the load, after the voltage falls below a certain value called as the 'Valley Voltage', the line current does not flow anymore. Instead, the capacitors discharge and provide the load current, thereby ensuring continuity of supply.
The Valley Fill PFC is as follows.

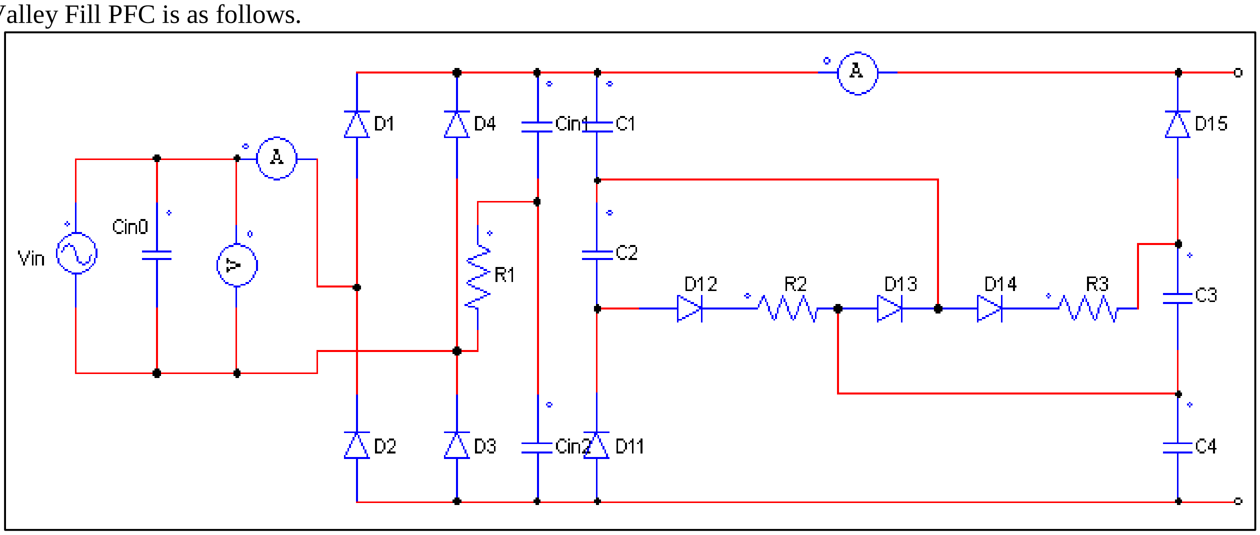


Fig. 1: Valley Fill Circuit diagram

Fig. 1 shows the proposed circuit. The circuit is inserted between the bridge-diode rectifier and the load. After the rectifier, there is the Valley fill circuit consisting of 5 diodes, 4 capacitors, and 2 resistors.
The circuit operation is divided into 5 stages.

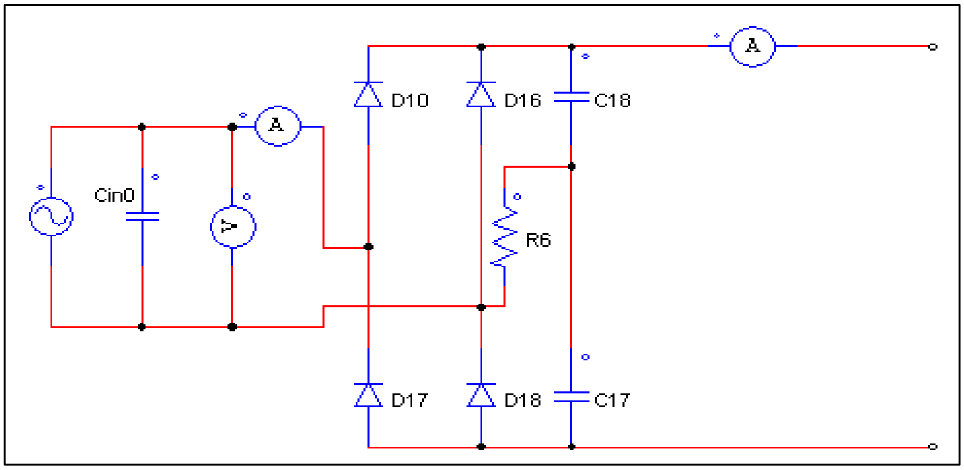


Fig. 2: During Stage 1

1) Stage 1: The line voltage is slightly higher than the valley-fill voltage (i.e. VC1 +VC2; VC3 +VC4 or VC1 + VC4) and the bridge diodes conduct. Input current flows to the output load directly. (Note: Vcx means voltage across capacitor CX, for X equals 1, 2, 3 or 4.)
2) Stage 2: The line voltage continues to rise and go slightly above the voltage sum, VC1 + VC3 + VC4 or VC1 + VC2 + VC4, the capacitor pair with lower voltage, or smaller capacitance, will be charged up fist. If C2 > C3, charging current will flows through C1-D14-R3-C3-C4 until.

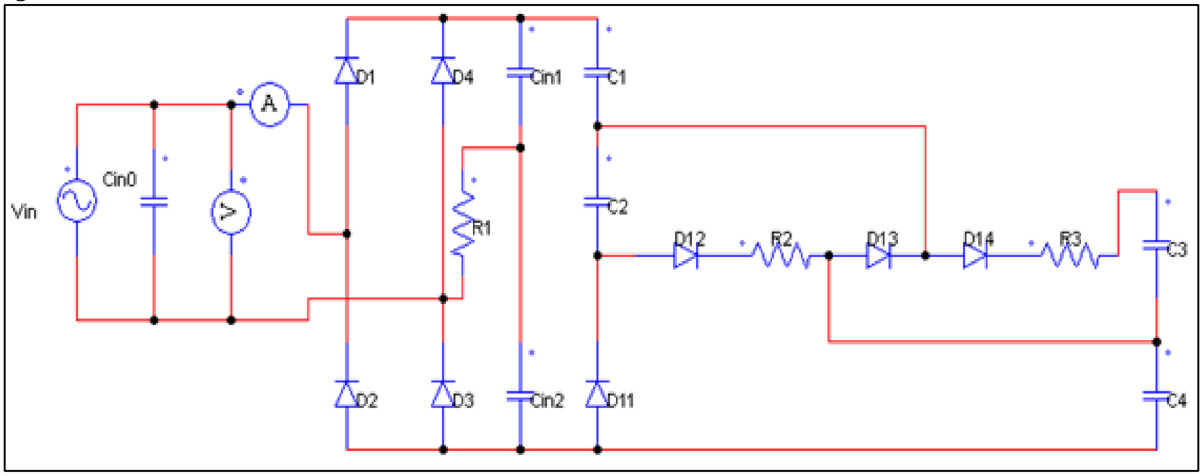


Fig. 3: During Stage 2

C3 voltage is equal to C2 voltage. Then C2 and C3 are charged in parallel. If C2 < C3, C2 will charge up first, and if C2 = C3, they will start charging up at the same time. The input current charges the capacitors as well as flows to the load.

3) Stage 3: The input current flows to the load only since all capacitors are fully charged. Unlike the conventional large bulk capacitor for which once it has been fully charged it will stay at the peak input voltage and the input current ceases flowing as the input voltage is decaying, the input current can still flow to the load in this circuit because the valley-fill voltage stays around two-third of the peak input voltage, assuming the capacitance are large enough to hold the output voltage. Thus the conduction time for bridge diodes are lengthened compared to the conventional rectifier.

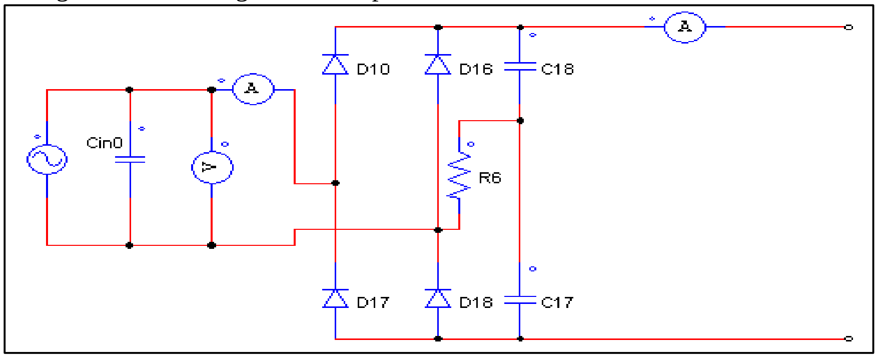


Fig. 4: Stage 3

4) Stage 4: When the input voltage decreases and falls below two-third of the input peak voltage or the voltage that VFPFC stays, the input current stops flowing because the bridge diodes are reversed biased. Instead, the capacitors pairs discharge in series to provide the output current. Again, depending on the capacitance of the capacitors pair, the one with smaller capacitance will discharge first.

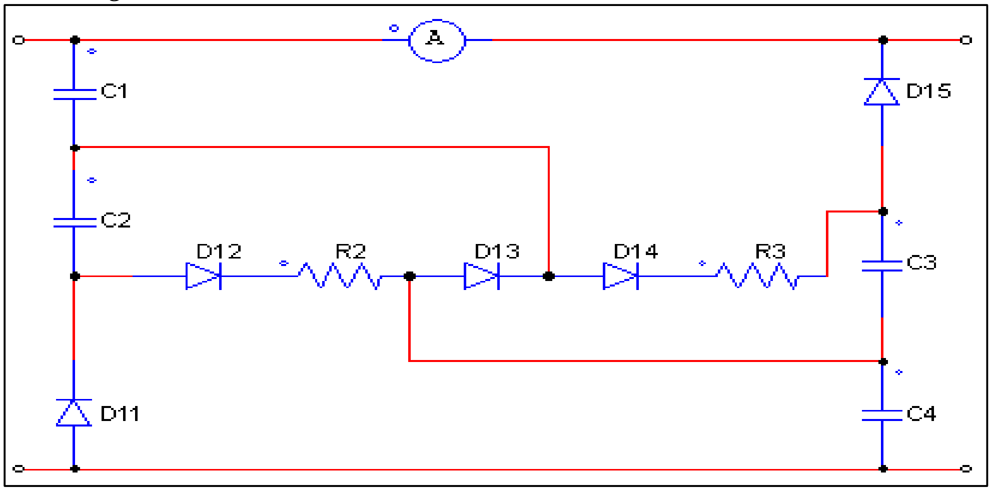


Fig. 5: Stage 4

5) Stage 5: Line voltage changes direction but is lower than the valley-fill voltage. However, input current still flows through the path R1-CIN2-D2. The charging/discharging cycle repeats at the next half line cycle when the input voltage is higher than the voltage sum of VC1+VC2, VC3+VC4 or VC1+VC4.

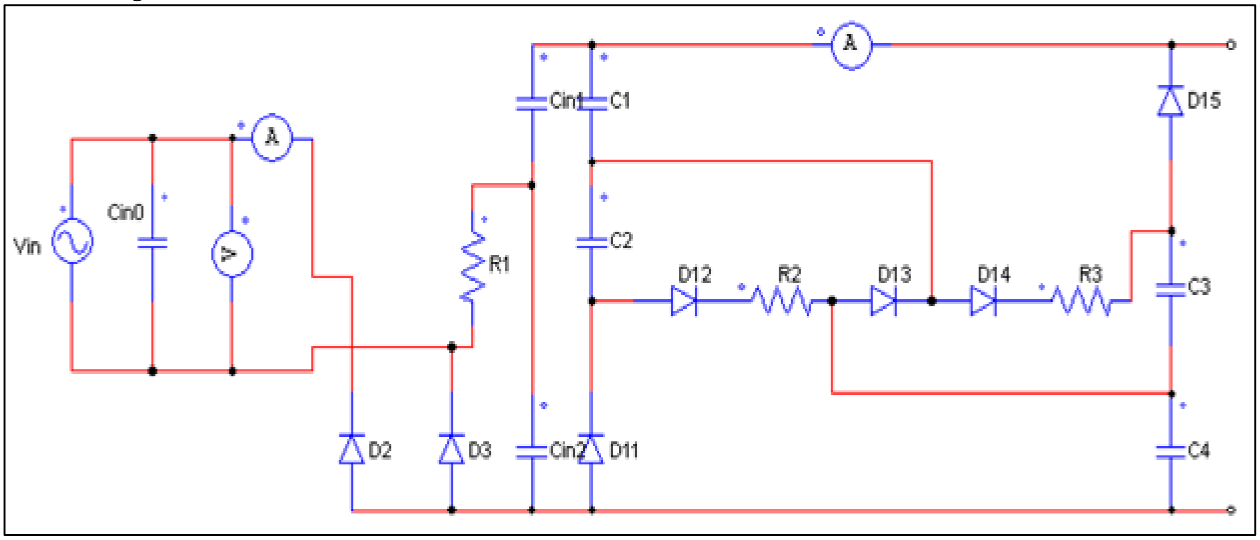
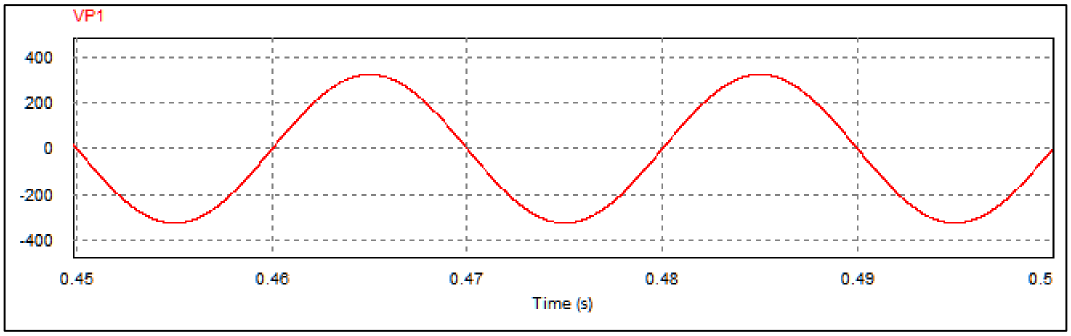


Fig. 6: Stage 5

III. Simulation and Experimental Results



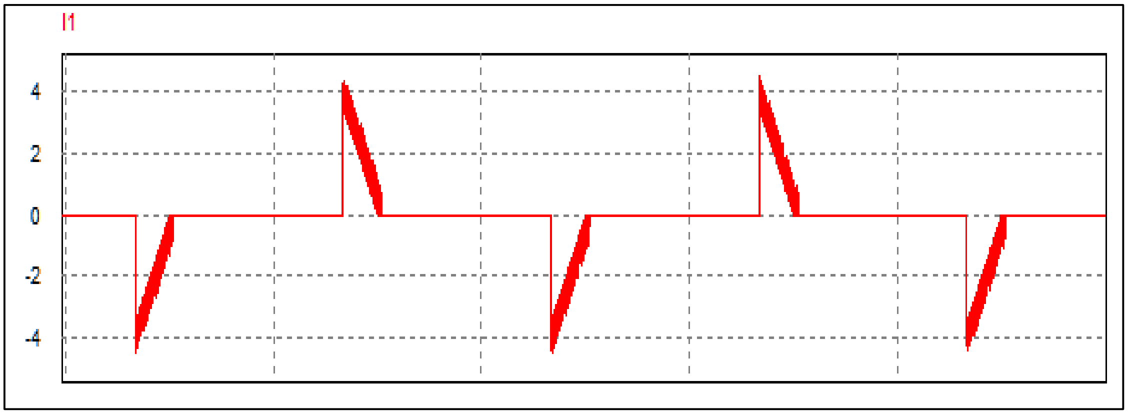


Fig. 7: Simulation Result: Voltage and Current waveforms without using VFC in the circuit

The waveforms show that during each half cycle, the load draws current in the form of pulses of short time period. It shows a poor power factor. The power factor in this case is 0.4 only.

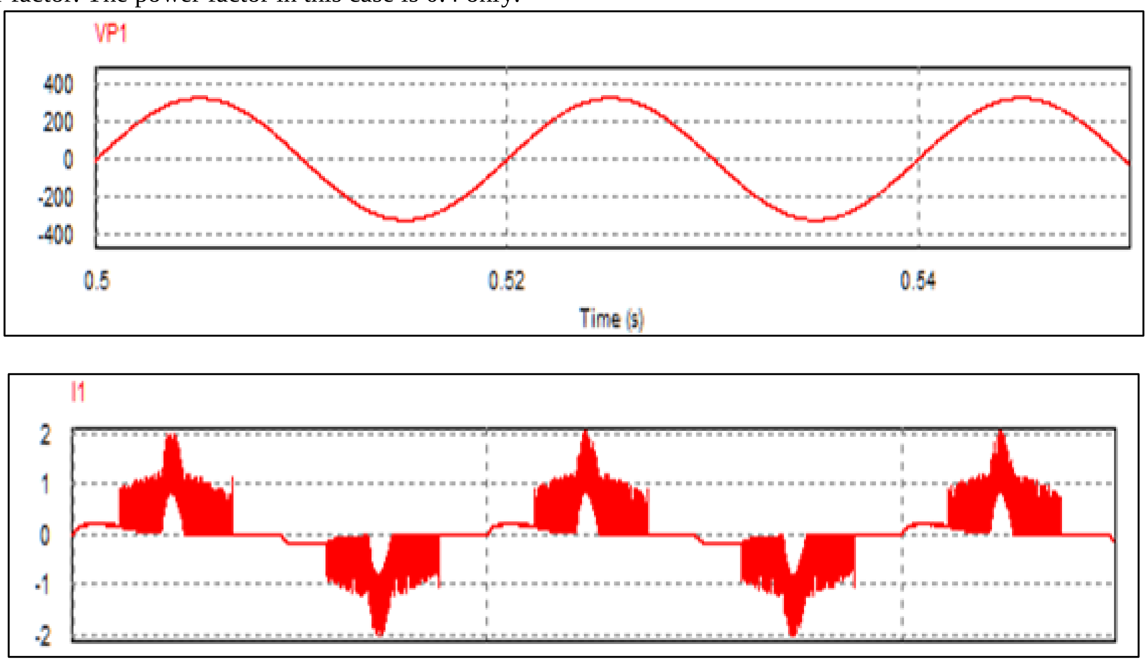


Fig. 8: Simulation Result: Voltage and Current waveforms after using VFC in the circuit

The simulation results show that after using VFPFC, the current waveform improves and comer nearer to sinusoidal for a better power factor which is attained as 0.75.

Simulation Hardware

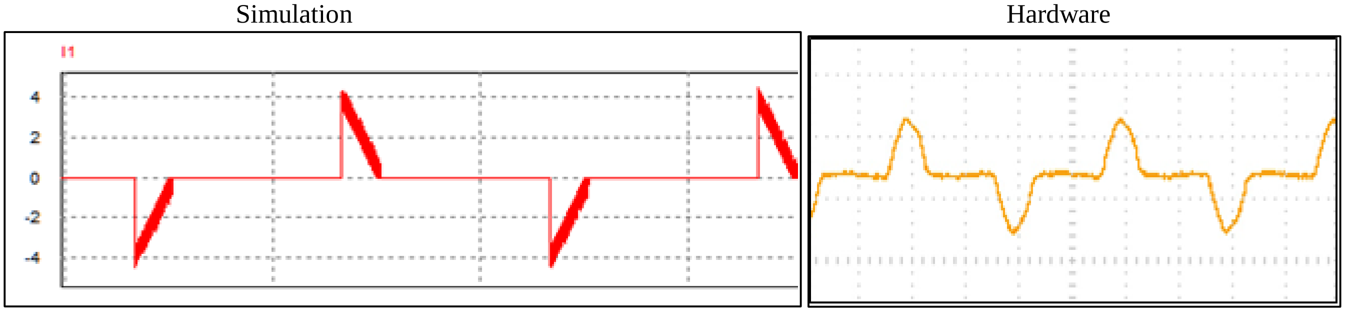


Fig. 9: Input current without VFC waveform

Simulation Hardware

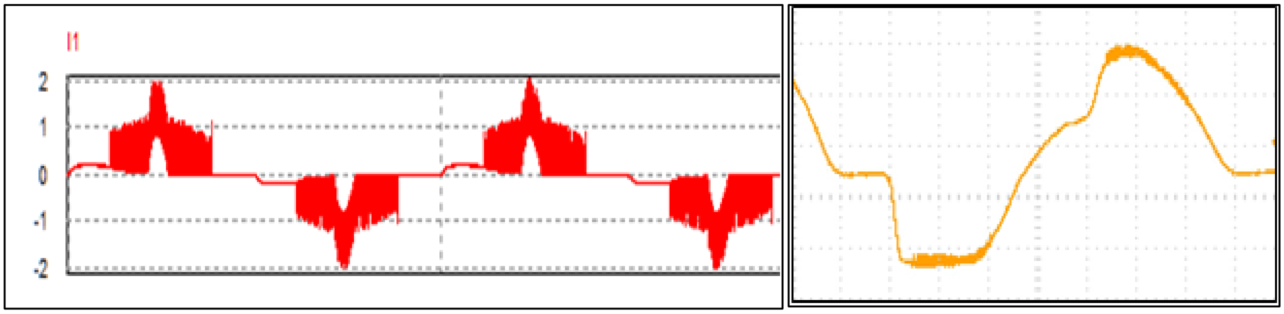


Fig. 10: Input current with VFC waveform

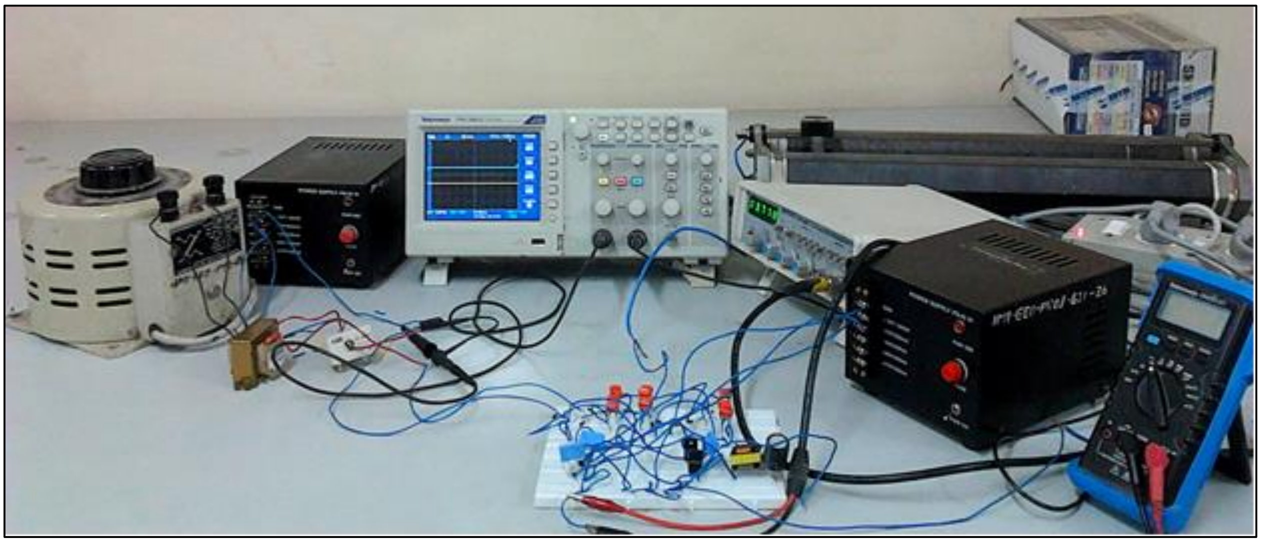


Fig. 11: The experimental setup

IV. CONCLUSION

The main objective of the paper is to analyze the working of valley fill circuit for power factor improvement. The valley fill circuit is analyzed by doing simulation and experimental results. It is evident that power factor is improved from 0.4 to 0.7 by using low cost valley fill circuit.

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