Design and Implementation of Viterbi Encoder and Decoder on FPGA

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Abstract

Our project deal with designing and implementing a convolutional encoder and Viterbi decoder which are the essential block in digital communication systems using FPGA technology. Convolutional coding is a coding scheme used in communication systems including deep space communications and wireless communications. It provides an alternative approach to block codes for transmission over a noisy channel. The block codes can be applied only for the block of data. The convolution coding has an advantage over the block codes in that it can be applied to a continuous DataStream as well as to blocks of data. The motivation of this paper is to understand a Viterbi decoder by Xilinx 12.4i tools.

Keywords: Convolution Encoder, Trellis Diagram, VHDL, Veterbi Decoder, FPGA

I. INTRODUCTION

Elias presented convolutional codes in 1955. Convolution coding has been utilized as a part of correspondence frameworks including profound space correspondence and remote correspondence. Leeway of convolutional coding is that it can be connected to a ceaseless information stream and in addition piece of information. Convolutional coding plan relates data components by method for selective - or (XOR) operation, bringing about the increments of transmission redundancy. Convolutional codes are utilized as a part of uses that require great execution with low usage cost. A few commonsense techniques have been produced for deciphering. In 1967 A.J Viterbi presented "Viterbi decoding" in view of the most extreme probability calculation. At the recipient, the real got encoded information in addition to the commotion is contrasted and the encoded information arrangement for each of the conceivable yields of the convolution encoder. The nearest speculative encoded information succession will be ideal gotten encoded information sequence. Viterbi calculation is the most asset expending, productive and hearty.

II. CONVOLUTION ENCODING

Encoding of convolutional codes can be expert utilizing straightforward registers. In convolutional encoder, the message stream constantly goes through the encoder dissimilar to in the piece coding plans where the message is initially separated into long squares and afterward encoded. Along these lines the convolutional encoder requires almost no buffering and capacity hardware [3]. In this paper for a convolutional encoder, the accompanying documentations are utilized c= number of output bits, x = number of bits entering at a time, m= number of stages of shift register, L= number of bits in a message sequence, j = number of modulo 2 adders.

A convolutional encoder is a Mealy machine, where the output is a function of the current state and the current input. It consists of one or more shift registers and multiple XOR gates. The stream of information bits flows in to the shift register from one end and is shifted out at the other end. XOR gates are connected to some stages of the shift registers as well as to the current input to generate the output. There is no theoretical basis for the optimal location of the shift register stages to be connected to XOR gates. It is based on an empirical approach. The location of stages is determined by the interconnection function. The location of stages as well as the number of memory elements determines the minimum Hamming distance. Minimum Hamming distance determines the maximal number of correctable bits. Interconnection functions for different rates and different number of memory elements and their minimum Hamming distances are available.

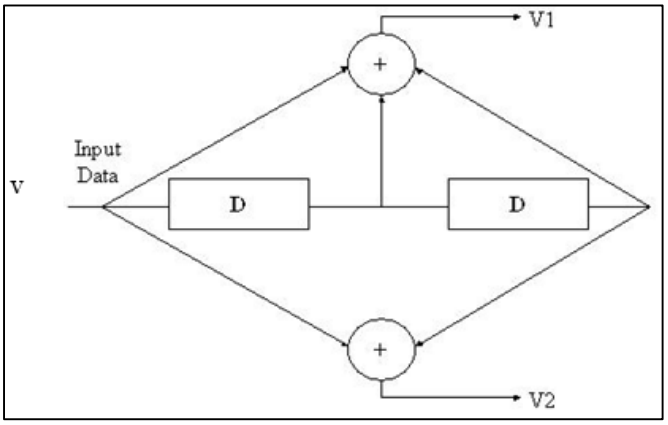

Fig. 1: Convolution encoder

The operation of a convolutional encoder can be simply understood with the help of a state diagram. Figure 1.2 represents the state diagram of the encoder shown in Figure 1.1. Figure 1.2 depicts state transition and the equivalent encoded outputs. As there are two memory-elements in the circuit, there are four probable states that the circuit can assume. These four states are represented as S0 through S3. Each state's information (i.e. the contents of flip-flops for the state) along with an input generated an encoded output code. For each state, there can be two outgoing transitions; one corresponding to a '0' input bit and the other corresponding to a '1' input bit.

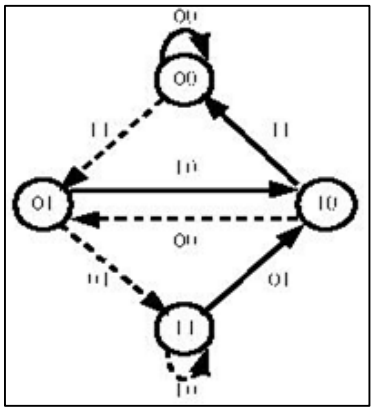

Fig. 2: State Diagram

The encoding for the sequence 0 1 1 0 1 0 0 and the output sequence is 00 11 00 01 01 11 10 is shown in the Figure 2.5.

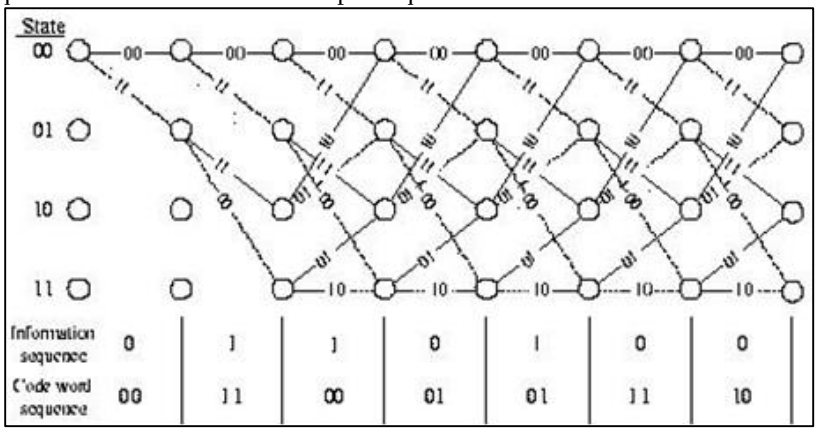

Fig. 3: Trellis Diagram for Encoder

III. VITERBI DECODING

The Viterbi decoding algorithm is a decoding process for convolutional codes for a memory-less channel. Figure depicts the standard flow of information over a noisy channel. For the intention of error recovery, the encoder adds surplus information to the original information i, and the output t is transmitted through a channel. Input at receiver end (r) is the information with redundancy and possibly, noise. The receiver try to remove the original information through a decoding algorithm and generate an

approximation (e). A decoding algorithm that maximize the prospect p(r|e) is a maximum likelihood (ML) algorithm. An algorithm which maximizes the p(e|r) through the proper selection of the estimate (e) is called a maximum a posteriori (MAP) algorithm. The two algorithms have the same results when the source information i has a uniform distribution.

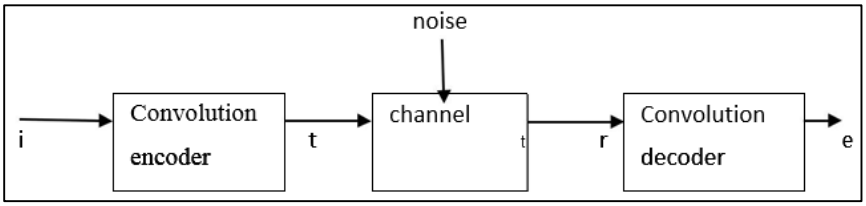

Fig. 4: Viterbi decoding algorithm

IV. IMPLEMENTATION OF VITERBI DECODER

The most important tasks in the Viterbi decoding algorithm are as follows:

1) Quantization: The analog input is converted into digital
2) Synchronization: recognition of the boundaries of frame and code symbols.
3) Branch metric calculation.
4) State metric update: Update the state metrics using the new branch metric.
5) Survivor path recording: Tag the surviving path at each node.
6) Output decision generation: Generation of the decoded output sequence based on the survivor path information. Figure illustrate the flow of the Viterbi decoding algorithm, which perform the above tasks in the precise order.

This segment discusses the various parts of the Viterbi decoding process. Analog signals are quantized and changed into digital signals in the quantization block. The synchronization block detects the frame boundaries of code words and symbol boundaries. We assume that a Viterbi decoder receives successive code symbols, in which the boundaries of the symbols and the frames have been identified.

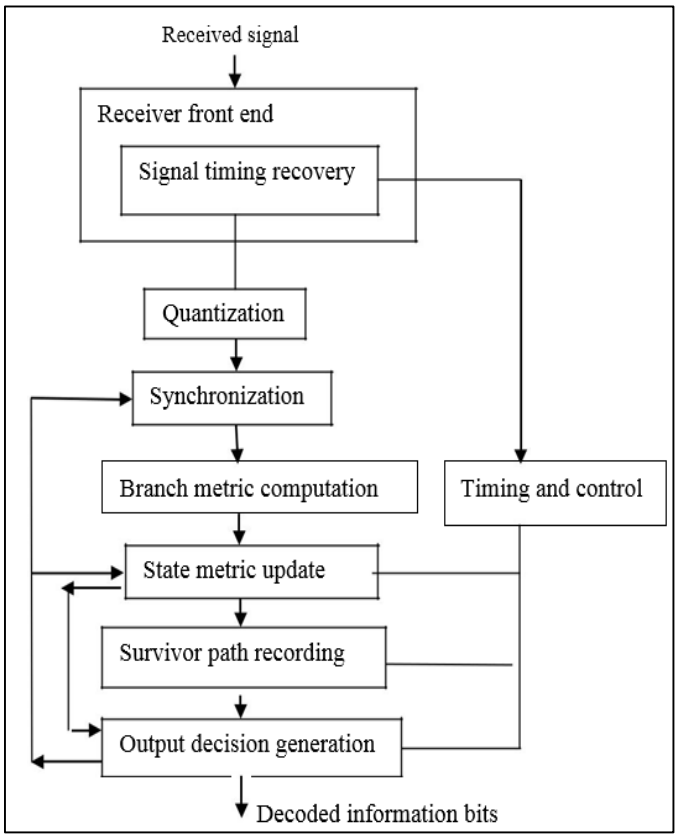

Fig. 4: Viterbi Decoder Flowchart

V. RESULT

The convolution encoder and viterbe decoder has been developed and the result is shown in figure below Input = 0110100
Output = 00110001011100

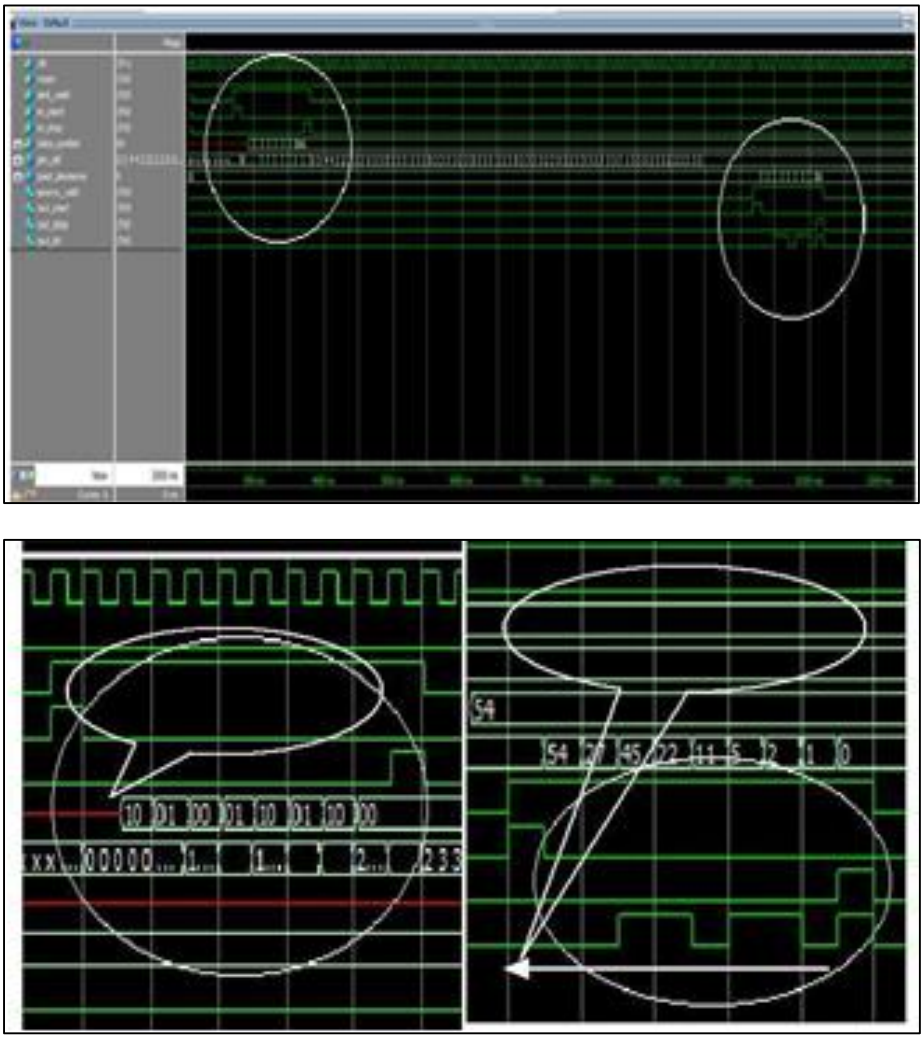

Fig. 5: Result

VI. CONCLUSION

Viterbi encoder and decoder for constraint length 7 and bit rate 1/2 is implemented using VHDL, simulated using Model sim PE student Edition and synthesis is done by Xilinx ISE Design suit. The working of the design is demonstrated for many trial with introducing errors. In this project few modifications are included in the general veterbi decoder algorithm,in order to make system more faster and accurate and also to reduced noise at the receiving end.

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