Multilevel Inverter with Reduced Number of Switches using Multi Carrier Phase Opposition Disposition PWM

Manu Jacob T 
PG Scholar
Department of Electrical & Electronics Engineering
Federal Institute of Science and Technology Angamaly, India

Sreeja E A
Assistant Professor
Department of Electrical & Electronics Engineering
Federal Institute of Science and Technology Angamaly, India

Abstract

Multilevel inverter is one of the attractive topology for dc to ac conversion. Multilevel inverter synthesizes desired voltage wave shape from several levels of DC voltages. Though multilevel inverter has a number of advantages it has drawbacks in the vein of higher levels because of using more number of semiconductor switches. This may leads to vast size and price of the inverter increases and also leads to complex control. The new multilevel inverter with reduced number of switches overcome this problem and is well suited for high power applications. Multi carrier PWM technique is used for sine wave generation. PODPWM with optimization of carrier using absolute sine reference signal is used for control.

Keywords: Multi Carrier Phase Opposition Disposition, PWM

I. INTRODUCTION

Power inverter is an electrical power device which is used to convert direct current (DC) into alternating current (AC). Using few control circuits and switches, one can get AC at any required voltage and frequency. Inverter plays exactly the opposite role of rectifiers as rectifiers are used for converting alternating current (AC) into direct current (DC). Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. Multilevel inverter is widely used in high power applications such as large induction motor drives, UPS systems and Flexible AC transmission Systems. Desired output can be obtained from several levels of input DC voltage sources and also the output levels depends on the number of input DC voltage sources. The multilevel inverters over several advantages over a conventional two level inverters such as lower semiconductor voltage stress, better harmonic performance, low Electro Magnetic Interference (EMI) and lower switching losses. The main drawback in Conventional cascaded multilevel inverter is that when levels are increasing it requires more number of semiconductor switches. This increases the inverter size and makes the control scheme more complex. Multilevel inverter with reduced number of switches reduces inverter size and makes the control less complex. The Diode clamped, Flying capacitor, Cascaded H-bridge inverter are the three main different multilevel inverter structures which are used in industrial applications with separate dc sources. In flying capacitor and diode-clamped inverter there is a problem of capacitor voltage balancing and this problem is overcome in cascaded H-bridge inverter. Conventional cascaded seven level multilevel inverter require twelve switches and three dc sources separately. The main drawback in Conventional cascaded is that when levels are increasing it requires more number of semiconductor switches. As a result some alternations are to be made inorder to reduce the size and switch of the inverter

II. NOVEL MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES

The novel topology of multilevel inverter with reduced number of switches can be used for different levels of output. The number of output voltage levels changes with number of switches and DC sources. The generalized expression for the number of switches is given by and the number of dc sources for the proposed topology is given by $v = \frac{n+1}{2}$ Where N= number of levels and $v=\frac{n+5}{2}$ Where S=number of dc voltage sources.
III. SEVEN LEVEL INVERTER WITH SIX SWITCHES AND THREE DC SOURCES

The figure 1 shows the novel seven level inverter topology with three dc sources and six switches. It is simple in design compared to the existing topologies. It also have additional features like only two switches conducting at an interval of time. Two switches used for polarity reversal and the remaining four switches used for waveform generation.

![Fig. 1: Novel seven level inverter](image)

Table 1

<table>
<thead>
<tr>
<th>Voltage level</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>S6</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>+Vdc</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>+2Vdc</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>+3Vdc</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>-Vdc</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-2Vdc</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-3Vdc</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

IV. NINE LEVEL INVERTER WITH SEVEN SWITCHES AND FOUR DC SOURCES

The figure 2 shows the novel nine level inverter topology with four dc sources and seven switches. It is simple in design compared to the existing topologies. It also have additional features like only two switches conducting at an interval of time. Two switches used for polarity reversal and the remaining five switches used for waveform generation. Figure 2 shows the circuit arrangement of novel topology of nine level inverter which consists of seven switches, four DC sources and the resistive load. Switches S6 and S7 are used for reversal polarity and the remaining switches are used to generate the levels in both positive and negative sides to produce the desired seven level waveforms. The switching states are given in the table 2.
PODPWM Control with Carrier Optimization

Phase Opposition Disposition (Pod) pulse width modulation is employed for control of switches. With the PODPWM method the carrier waveforms above the zero reference value are in phase. Using multi carrier phase opposition disposition pulse width modulation, seven level inverter requires six carriers to be compared with sinusoidal reference signal and nine level inverter requires eight triangular carrier waves to be compared with sinusoidal reference signal. The optimization of multi carrier phase opposition disposition PWM is done by taking the absolute or positive value of the modulating reference sine wave. This method of optimization of PODPWM using absolute sine reference wave reduces the number of carriers to half as shown in figure 3.
Multilevel Inverter with Reduced Number of Switches using Multi Carrier Phase Opposition Disposition PWM

![Image](image.png)

Number of carriers required for n level = $\frac{n-1}{2}

Modulation index $M = \frac{A_{ref}}{2 \times A_{tri}}$

$A_{tri}$ is the amplitude of triangular wave, n is the number of levels of inverter. By optimization the number of triangular carriers required for seven level inverter reduces to three and the number of triangular carriers required for nine level inverter reduces to four.

V. SIMULATION STRATEGY AND RESULTS

The novel topology of seven level inverter consists of six switches and three DC sources. The figure 4 shows simulation circuit diagram of novel seven level inverter with seven switches and four DC sources.

![Fig. 4: Simulation Circuit](image.png)

The figure 5 shows the output of the nine level inverter with four DC Sources of 6 V and seven switches. The simulation results shows the nine levels of the output voltage. The THD is obtained as 4.58 % by FFT analysis in simulation and is shown in the figure 6.

![Fig. 5: Output Voltage across Load](image.png)
A new topology for seven level multilevel inverter and nine level inverter is designed and the simulations are done in Matlab/Simulink for nine level inverter. The simulation results across the load with nine levels are obtained. THD is obtained as 4.58%. Optimized phase opposition disposition pulse width modulation is used. Number of carriers required reduced to half.

REFERENCES


