An Unbalanced voltage Compensation Strategy 
for Islanded Microgrids by using Fuzzy Logic Controller

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Abstract

In this paper, a control technique with low bandwidth transmission correspondences for paralleled three-phase inverters is proposed to accomplish palatable voltage unbalance compensation. The proposed control calculation principally comprises of voltage/current impedance loop controllers, a droop controller, a particular virtual impedance loop, and an unbalance compensator. The inward circle controllers depend on the stationary reference frame to better alleviate the voltage mutilation under nonlinear loads. Droop control and particular virtual impedance loop accomplish exact current-sharing when supplying both linear and nonlinear loads. In addition, by altering voltage references concurring to the adequacy of the negative sequence voltage, the unbalance component, which is for the most part created by single phase generators/loads, can be alleviated to an extreme low value. At last, an AC microgrid which incorporates three-phase three-leg inverters was tried to accept the proposed control technique.

**Keywords:** Microgrids, voltage unbalance compensation, virtual impedance, droop control

I. INTRODUCTION

As of late, dispersed energy resources (DERs, for example, wind turbines, photovoltaic systems and small scale turbines, have pick up an incredible expanding enthusiasm since they are monetary and environment amicable. When all is said in done, power electronic converters are utilized as interfaces amongst DERs and the grid [1], to such an extent that electrical power with great quality and high dependability can be conveyed to the heap or utility grid, as appeared in Fig. 1. This paper concentrates on islanded microgrids where the interfacing converters for the most part work as voltage sources to take an interest on the voltage and frequency direction while sharing at the same time active and reactive power precisely by conforming output voltage phase angles. Be that as it may, it is too favored that those converters could give power quality administration capacity, in a manner that we can take full utilization of the converters accessible limit. It is outstanding that power quality issues, particularly voltage/current unbalances and voltage/current distortions have turned out to be increasingly genuine in cutting angle power system. For example, in islanded microgrids, the voltage unbalance issue is a notable issue basically created by the utilization of single-phase generators/loads and it can lead to insecurity and power quality issues. Keeping in mind the end goal to improve the voltage waveform quality, a few segments to manage the voltage unbalance compensation have been produced.

![Fig. 1: General architecture of a microgrid.](image-url)
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II. LOCAL CONTROLLER DESIGN

Fig. 2: Implementation of the local controllers.

Fig. 3: Small signal model of single inverter.

Fig. 2 defines the control methodology of inverter local controllers. LCL filter is received here, however it really works as a conventional LC filter with a coupling inductor. The fundamental capacity of the system side inductor is to optimize the dynamic execution and to shape the output impedance. Likewise its current is measured for power estimation and virtual impedance which will be clarified later.
A. Inner Loop Design

It can be seen from Fig. 2 that the inner loops are actualized in two-phase stationary frame and all the measured voltage and current are changed from abc to αβ coordinates, in this manner the computational weight is diminished essentially. Both voltage and current controllers depend on proportional resonant (PR) controller rather than the conventional proportional integrator (PI) controller. The reason is that PR controller can give limitless addition at the chosen resounding frequency to give agreeable following execution. At the end of the day, the execution of PR controller at chose resounding frequency is conceptually similar to the execution of PI controller at 0Hz. Likewise, keeping in mind the end goal to relieve the voltage and current distortion under nonlinear loads, the PR controllers are tuned at central frequency, third, fifth, seventh, ninth and eleventh order harmonics.

Displaying of the main power circuit and the inner loop controller in synchronous reference frame is set up here to acquire the closed loop transfer capacity. By utilizing abc/αβ transformation in the power plant and neglecting the zero quadrature segments, the three phase inverter can be communicated as a decoupled two phase system. Fig.3 demonstrates the small signal model of the decoupled two phase system. It is commendable taking note of that one and only inverter is portrayed here to rearrange the figure. As per the small signal model, the control plan can be portrayed in Fig. 4. The closed loop exchange capacity is derived in (1):

\[
v_c(s) = v^*_{o}(s) - Z_o(s)v^*_{ref}(s) = \frac{G_v(s)G_i(s)G_{PR}(s)}{LC^2 + CG_v(s)G_{PR}(s)s + G_v(s)G_i(s)G_{PR}(s)s + 1}v^*_{ref}(s) - \frac{L_i + G_v(s)G_{PR}(s)}{LC^2 + CG_v(s)G_{PR}(s)s + G_v(s)G_i(s)G_{PR}(s)s + 1}i_o(s)
\]

where \(v_c(s)\) is the capacitor voltage, \(v^*_{o}(s)\) is the open circuit voltage, \(i_o(s)\) is the output current, \(Z_o(s)\) is the equivalent output impedance, \(v_{ref}(s)\) is the voltage reference, \(L\) is the converter side inductor, \(C\) is the filter capacitor. \(G_v(s), G_i(s)\) and \(GPWM(s)\) are the transfer capacity of voltage controller, current controller furthermore, PWM delay, individually. Their transfer capacity can be communicated as:

\[
G(s) = k_{ip} + \sum_{b=1,3,5,7,9,11} k_{ip}b^2 \frac{s}{s^2 + (b\omega)^2}
\]

\[
G(s) = k_{ip} + \sum_{b=1,3,5,7,9,11} k_{ip}b^2 \frac{s}{s^2 + (b\omega)^2}
\]

\[
GPWM(s) = \frac{1}{1 + 1.5T_s s}
\]

Fig. 4: Equivalent control block diagram of the inverter.
where \( k_{vp} \) and \( k_{hr} \) are the relative coefficients and resonant coefficients (first, third, fifth, seventh, ninth and eleventh) of voltage controller separately. \( k_{ip} \) and \( k_{hir} \) are the relative coefficients and resonant coefficients (first, third, fifth, seventh, ninth and eleventh) of current controller separately; \( \omega \) is the fundamental angular frequency while \( T_s \) is the sampling time. Fig. 5 defines the Bode plot of the inverter closed loop transfer function by utilizing diverse arrangement of parameters. As it can be seen, the addition of the closed loop transfer function at basic frequency and third, fifth, seventh, ninth, eleventh order harmonics is solidarity while the increases at different frequencies hold at a generally lower esteem. Along these lines, the output voltage can track the reference correctly.

### B. Droop Control Implementation

Keeping in mind the end goal to avoid circling currents among the parallel inverters without utilizing communication link between them, droop control is received in this paper. To better represents droop control theory, accepting two inverters associated in parallel and sharing loads at the regular node. The proportional circuit is appeared in Fig. 6. From Fig. 6, the active power \( P \) and reactive power \( Q \) infused by every DG can be express in (5) and (6), separately.

\[
P_i = \left( \frac{E_i}{Z_i} \right) \cos \phi_i - \left( \frac{E_i}{Z_i} \right)^2 \sin \phi_i \cos \theta_i + \frac{E_i}{Z_i} \sin \phi_i \sin \theta_i \tag{5}
\]

\[
Q_i = \left( \frac{E_i}{Z_i} \right) \sin \phi_i - \left( \frac{E_i}{Z_i} \right)^2 \cos \phi_i \sin \theta_i + \frac{E_i}{Z_i} \cos \phi_i \cos \theta_i \tag{6}
\]

Where \( E_i \) and \( \phi_i \) are the amplitude and the phase angle of the output voltage of the every inverter, \( Z_i \) and \( \theta_i \) are the abundancy what's more, phase point of the line impedance of every inverter, separately. \( V \) is the voltage adequacy of normal AC transport. Note that phase angle of regular AC bus voltage is taken as the phase reference. When all is said in done, the line impedance is for the most part inductive, i.e. 90° \( \leq \theta \leq 90° \). Besides, accepting the phase difference \( \phi_i \) between inverter voltage and AC bus voltage is little enough, so that \( \sin \phi_i \) can be around equivalent to \( \phi_i \) and \( \cos \phi_i \) can be roughly equivalent to 1. At that point, from (5) and (6), the accompanying approximations can be gotten:
From (7) and (8), it can be seen that active power $P_i$ is prevailing by phase angle $\varphi_i$ while reactive power is for the most part depend on inverter voltage $E_i$. At that point, a artificial droop is acquainted here with modify the frequency and amplitude of the output voltage dynamically:

$$\varphi^* = \varphi_0 - \left( m_p - \frac{m_I}{s} \right) \left( P^* - P_{+}^{\text{ref}} \right)$$  \hspace{2cm} (9)

$$E^* = E_0 - n_p \left( Q^* - Q_{+}^{\text{ref}} \right)$$  \hspace{2cm} (10)

where $\varphi^*$ and $E^*$ are the amplitude and phase angle of the output voltage reference while $E_0$ and $\varphi_0$ are the sufficiency and phase angle of the output voltage at no load condition, $P^+$ and $Q^+$ are the instantaneous fundamental positive sequence active and, reactive power, separately, and $P_{+}^{\text{ref}}$ and $Q_{+}^{\text{ref}}$ are the reference of essential positive sequence active and reactive power, separately; $m_p$ and $m_I$ are the corresponding and indispensable coefficients of active power controller, separately. $m_l$ principally impact the dynamic normal for the system since it includes inactivity to the system; $n_p$ is the necessary coefficients of reactive power controller. It can be seen from (7)-(10) that the higher the droop coefficients is, the better power sharing can be accomplished. Be that as it may, the voltage and frequency deviation will likewise gotten to be bigger when the droop coefficients get to be greater. This tradeoff can be remunerated by presenting auxiliary controller, as delineated in [10]. Subsequently, both the corresponding coefficients should to be carefully chosen by and (12):

$$m_p = \frac{\Delta f}{P}$$  \hspace{2cm} (11)

$$n_p = \frac{\Delta E}{Q}$$  \hspace{2cm} (12)

Where $\Delta f$ and $\Delta E$ are the maximum allowable deviation of frequency and abundance from its ostensible worth, individually. $P$ and $Q$ are the evaluated active and reactive power, individually. A positive-negative-sequence symphonious voltage/current part extractor [11-12] in view of a second-order generalized integrator (SOGI) is actualized to help the droop controller and the virtual impedance loop, which will be presented in Section C. Since the key positive sequence part extraction is just about the same with that of the key negative sequence and music, just the key positive sequence voltage extractor is appeared here in Fig. 7.

![Fig. 7: Fundamental positive sequence component extractor.](image-url)
Fig. 8 defines the execution block diagram of the droop controller. The power calculation block, based on the quick reactive power theory, is trailed by a low pass filter with a 2 Hz cut-off frequency, so that the power wavering can be filtered out.

### Virtual Impedance Loop

So as to share the power correctly between the appropriated inverters, the output impedance of the inverter must be re-intended to mitigate the impact of control parameters what's more, line impedance on the power sharing accuracy. Here, (1) can be reworked as:

$$v_i(s) = G(s)v_{ref}(s) - Z_0(s)\cdot i_o(s)$$

(13)

where $G(s)$ speaks to the close loop transfer function of the inverter, and $Z_0(s)$ speaks to the close loop output impedance of the inverter. From the above condition, a two-terminal Thevenin equal circuit of the close loop inverter can be gotten, as appeared in Fig. 9.

![Virtual Impedance Loop Diagram](image)

Fig. 9: Thevenin equivalent circuit of the close loop inverter.

On the off chance that no control loop is actualized to repay the output impedance, the amplitude of the output impedance at principal frequency and third, fifth, seventh, ninth and eleventh order harmonics is extremely small, as demonstrated the blue bend in Fig. 10. Therefore, a virtual impedance loop must be included the control block to settle the output impedance.

![Bode Plot of Output Impedance](image)

Fig. 10: Bode plot of the output impedance.
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Since the droop law in this paper is ensured just when the output impedance is profoundly inductive. Along these lines, a positive sequence virtual inductor \( L^+ \) is added to make the output impedance more inductive, so a superior decoupling of P and Q can be guaranteed. The motivation behind including the positive-sequence virtual resistor \( R^+ \) is to make the system more damped, so that the output current can be restricted inside a satisfactory extent. For principal negative grouping and every request of the music, a resistor is imitated at the output side to upgrade the sharing of nonlinear load sharing among the DGs. Contrasted and utilizing a real resistor, the virtual resistor has the favorable position of no power misfortunes and the likelihood to choose music and successions. The usage plan of the virtual impedance loop, which comprises of three fundamental parts, is represented in Fig. 11. The initial segment is central positive sequence virtual impedance loop, which just presents virtual resistor \( R^+ \) and virtual inductor \( L^+ \) to central positive sequence current. The second part is central negative sequence virtual impedance loop which presents virtual resistor \( R^- \) to crucial negative sequence current. The third part is harmonic virtual impedance loop which presents virtual resistor \( R_h \) to third, fifth, seventh, ninth and eleventh order harmonics, individually. Note that \( \omega \) is the nominal angular frequency of the system.

It is important that there is a tradeoff between the nonlinear current sharing accuracy and inverters output voltage contortion. This voltage bending begins from the voltage drop on the virtual impedances. In this way, the estimation of the virtual impedances must be chosen painstakingly to guarantee a well power sharing accuracy, and in the interim ensure the voltage Total harmonic Distortion (THD) is constrained in a satisfactory reach. What's more, voltage contortion brought on by virtual impedance is additionally the purpose behind isolating the virtual impedance of consonant and principal negative grouping part with crucial positive sequence part, so that the virtual impedance of critical negative sequence and consonant parts can be set to a bigger quality.

III. UNBALANCE COMPENSATOR DESIGN

In this paper, the voltage unbalance pay technique is enhanced as far as controlling the negative sequence voltage straightforwardly. As appeared in Fig. 2, the reference of voltage controller is the superposition of the output of unbalance compensator and droop controller. The scientific portrayal of the unbalance compensator executed in synchronous reference (dq) outline is appeared in (14):

\[
v_{cen} = \left[ \left| v_{ref} \right| - \sqrt{v_d^2 + v_q^2} \right] \cdot PI_1(s) - Q \cdot PI_2(s) \cdot \frac{v_d}{\sqrt{v_d^2 + v_q^2}}
\]

where \( v_{cen} \) is the control signal send to inverter local controller, \( |v|_{ref} \) is the reference of negative sequence voltage, \( Q^- \) is the negative sequence reactive power at purpose of normal coupling (PCC), \( v^- d \) and \( v^- q \) are the dq segments of negative sequence voltage separately, \( PI_1(s) \) and \( PI_2(s) \) are the negative sequence voltage controllers, individually. It can be seen that the voltage unbalance level is moderated by controlling the PCC voltage straightforwardly while the negative sequence reactive power infusion is controlled in a roundabout way. Point by point calculation of the unbalance compensator is portrayed in Fig. 12. As it can be seen, dq segments of the negative sequence voltage at PCC is initially removed by turning VPPC with negative angular frequency \(-\omega\) and after that took after by a low pass filter (LPF). Moreover, the abundancy of negative sequence voltage \( |v^-| \) is computed with sifted \( v^- d \) and \( v^- q \) and is thereafter send to a PI controller to produce the reference of negative sequence reactive power \( Q^-\)
ref. Another PI controller sustained with the mistake of $Q_{\text{ref}}$ and $Q_{\text{inv}}$ is executed here to upgrade the dynamic behavior of the unbalance compensator. At long last, the output of the PI controller is multiplied by standardized $v_{\text{ref}}$ and changed to $a\beta$ directions to create the compensation signal which is send to the voltage loop controller.

Fig. 12: Block diagram of the proposed unbalance compensator.

IV. FUTURE EXTENSION

A. Fuzzy Logic Controller:
A fuzzy control framework is a control framework in light of fluffy rationale—a numerical framework that investigates simple info values regarding sensible variables that interpretation of constant qualities somewhere around 0 and 1, as opposed to established or advanced rationale, which works on discrete estimations of either 1 or 0 (genuine or false, respectively).

B. Overview:
Fluffy rationale is broadly utilized as a part of machine control. The expression "fluffy" alludes to the way that the rationale included can manage ideas that can't be communicated as the "genuine" or "false" but instead as "incompletely genuine". Albeit elective methodologies, for example, hereditary calculations and neural systems can perform generally and additionally fluffy rationale as a rule, fluffy rationale has the point of interest that the answer for the issue can be thrown in wording that human administrators can see, so that their experience can be utilized as a part of the outline of the controller. This makes it less demanding to automate undertakings that are as of now effectively performed by humans.

V. SIMULATION RESULTS

A. After compensation:
Proposed method results:
1) Unbalanced voltage
2) \( V_{pcc} \)

3) \( I_{21} \)

4) \( V_{21} \)
5) \( V_{ll} \)

6) \( V_d \)

7) \( V_q \)
8. Extension results:

1) Unbalanced factor

2) Vpcc

3) I21
4) V2/I

5) V1/I

6) I/I
C. THD’S Comparison for extension and proposed method:

1) II1 THD under Proposed Method

![Image of THD analysis for proposed method]

2) II1 THD under Extension

![Image of THD analysis for extension method]
3) I21 proposed THD

![I21 proposed THD graph]

4) I21 THD under extension

![I21 THD under extension graph]
5) V11 THD For proposed

![An Unbalanced voltage Compensation Strategy for Islanded Microgrids by using Fuzzy Logic Controller](image)

6) V11 THD for extension

![An Unbalanced voltage Compensation Strategy for Islanded Microgrids by using Fuzzy Logic Controller](image)
7) V21 proposed THD

![Image of V21 proposed THD](image1.png)

8) V21 extension THD

![Image of V21 extension THD](image2.png)
9) Vpcc Proposed THD

![An Unbalanced voltage Compensation Strategy for Islanded Microgrids by using Fuzzy Logic Controller (IJIRSTI Volume 4 / Issue 5/004)](image)

10) Vpcc extension THD

![An Unbalanced voltage Compensation Strategy for Islanded Microgrids by using Fuzzy Logic Controller (IJIRSTI Volume 4 / Issue 5/004)](image)

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Output Name</th>
<th>Proposed THD (%)</th>
<th>Extension THD (%)</th>
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<tbody>
<tr>
<td>1.</td>
<td>I11</td>
<td>25.33</td>
<td>17.42</td>
</tr>
<tr>
<td>2.</td>
<td>I21</td>
<td>25.33</td>
<td>17.42</td>
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<td>Vpcc</td>
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Table – 1
Results Comparison Table
VI. CONCLUSIONS

In this paper, a novel direct voltage unbalance compensation control procedure for islanded microgrids has been researched. The control structure incorporates two levels: a nearby controller and a direct voltage unbalance compensator. The local controller for the most part deals with the bus voltage regulation what's more, the power sharing exactness, while the direct voltage unbalance compensator adds to moderate the voltage unbalance at the PCC by controlling the voltage reference. The effectiveness of the control plan has been approved with three LCL DG converters associated in parallel sharing a basic AC transport. The exploratory results demonstrate that the negative sequence voltage can be all around stifled to the desired worth with a fulfilled load sharing accuracy.

REFERENCES