

FPGA Realization of Optimized Digital Down Converters for WCDMA and CDMA 2000

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Abstract

This paper aims to provide an efficient design of digital down converters (DDC) that are used in receiver section of software defined radios (SDR). SDR is a radio in which some or all of the physical layer functions are software defined, making it flexible, upgradable and reliable wireless communication structure. In digital signal processing (DSP), a digital down-converter, converts a digitized real signal centered at an intermediate frequency (IF) to a baseband complex signal centered at zero frequency. In addition to down conversion, DDC's typically decimate to a lower sampling rate. WCDMA and CDMA 2000 are some of the third generation applications of SDR and thus the implementation of optimized DDC structure for these applications is presented. The DDC is first designed in MATLAB Simulink tool (R2012B) and codes are generated using MATLAB. Then the verilog codes are written for the same structure using proposed SHIFT and MUX based multiplier. Both the designs are synthesized on Altera Cyclone II EP2C35F672C6 field programmable gate array (FPGA). The model built using proposed SHIFT and MUX based multiplier provides an area improvement of 77.01% and 78%, speed improvement of 26.73% and 27.05% for WCDMA DDC and for CDMA 2000 DDC respectively, making it suitable for SDR application.

Keywords: DDC, FPGA, SDR, SHIFT and MUX

I. INTRODUCTION

Software defined radios or SDRs, do have characteristics that make them unique from other types of radios. As the name implies, a SDR is a radio that has the ability to be transformed through the use of software or re-definable logic. Quite often this is done with general purpose digital signal processors (DSP) or field programmable gate arrays (FPGA). Although typical architectures implement waveforms in the digital domain using microcontroller units (MCU) and DSPs, today FPGAs have emerged as high performance programmable hardware to execute highly parallel, computationally intensive signal processing functions efficiently which enable SDR implementation. SDRs are ideal candidates to be used for multi-carrier, single-carrier, single-band, multiband and multi-mode transceivers. The key point is that SDRs have the ability to go beyond single channel, single mode transceiver technology with the ability to change modes arbitrarily because the channel bandwidth, rate, and modulation are all flexibly determined through software [1].

The main blocks of the SDR are the transmitter and receiver. The transmitter comprises of modulator and digital up converter which converts the baseband signals to IF analog signals and the receiver comprises of digital down converter and demodulator[2] – [8]. The Digital Down converter comprises of down samplers and filters. The process of down sampling followed by filtering is known as decimation. Various filter can be used to effectively design the decimator with each filter having its own advantages such as half band filters having smaller computations, less registers and short delay from its half zero coefficient [2], pulse shaping root-raised cosine (RRC) filters [9] and anti-aliasing cascaded- integrated – comb (CIC) filters [2].

For real time signal processing finite impulse response (FIR) filters with higher order must be employed due to the fact that the filter order determines the width of transition band [10]. Since FIR filter structure employs multipliers and adders, the number of multiply-accumulate (MAC) operations required per filter output increases linearly with the filter order, real-time implementation of these filters of large orders is a challenging task [11]. Several attempts have, therefore, been made and continued to develop low-complexity dedicated VLSI systems for these filters. In this paper we have used a new multiplier known as SHIFT and MUX based multiplier which has less complexities when compared to other distributed arithmetic (DA) and look-up table (LUT) based multiplier [10].

Since WCDMA and CDMA 2000 are the most popular third generation application of SDR, their DDC structures have been discussed here [12]. The filters used in the DDC must be able to obtain the required narrowband channels from the available wideband signal [13]. The DDC architecture is first realized in MATLAB (R2012B) Simulink tool and then the same DDC structure realization is optimized by using proposed SHIFT and MUX based multiplier. MATLAB codes generated for the

Simulink model and the codes written using SHIFT and MUX based multiplier are synthesized on Altera Cyclone II EP2C35F672C6 FPGA device. The comparison between these two implementation is done and it shows that the DDC implemented using SHIFT and MUX based multiplier provides significant optimized results.

The rest of this paper is organized as follows. section 2 gives the general view about DDC and the components involved, section 3 gives the specifications of CDMA 2000 and WCDMA and their detailed DDC block Diagram, section 4 provides the detailed description about how the proposed SHIFT and MUX based multiplier works, section 5 describes the DDC implementation and discussion on results obtained in Simulink environment and Altera FPGA, and section 6 provides the detailed conclusion of this paper.

II. DIGITAL DOWN CONVERTER

A DDC consists of a low-pass filter (LPF) and a down sampler, which may be integrated into the low-pass filter. The general block diagram of DDC structure is shown in Fig1. The input signal is the complex sinusoid at the intermediate frequency. Multiplication of the intermediate frequency with the input signal creates images centered at the sum and difference frequency.

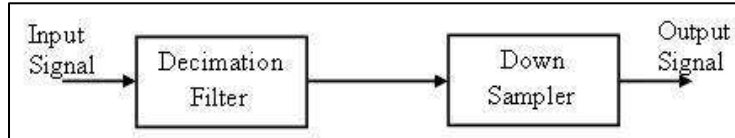


Fig. 1: DDC General Block Diagram

The low pass filters pass the difference (i.e. baseband) frequency while rejecting the sum frequency image, resulting in a complex baseband representation of the original signal. Assuming judicious choice of IF and LPF bandwidth, the complex baseband signal is mathematically equivalent to the original signal. In its new form, it can readily be down sampled and is more convenient to many DSP algorithms. It also performs decimation and matched filtering to remove adjacent channels and maximize the received signal-to-noise ratio (SNR). Any suitable low-pass filter can be used including FIR, IIR and CIC filters. The most common choice is a FIR filter for low amounts of decimation or a CIC filter followed by a FIR filter for larger down sampling ratios

A. Down Sampling

Down sampling is the process of removing zero-valued samples between original samples. If we down sample by a factor of L, then L-1 zeroes are removed between two samples. In other words, in signal processing, down sampling is the process of reducing the sampling rate of a signal. The down sampling factor is usually an integer or a rational fraction greater than unity. This factor multiplies the sampling time or, equivalently, divides the sampling rate.

B. Decimation

Decimation is the process of down sampling followed by filtering. The primary reason to decimate is to decrease the sampling rate at the output of one system. Since down sampling reduces the sampling rate, it is usually a good idea to make sure the Nyquist-Shannon sampling theorem criterion is maintained relative to the new lower sample rate, to avoid aliasing in the resulting digital signal. To ensure that the sampling theorem is satisfied, a low pass filter is used as an anti-aliasing filter to reduce the bandwidth of the signal before the signal is down sampled. The overall process (low-pass filter, then down sample) is called as decimation.

C. FIR Filter

In signal processing a finite impulse response (FIR) filter is a filter whose response is of finite duration, because it settles to zero in finite time. Fig 2 shows a discrete-time FIR filter of order N. For this filter, the output is a weighted sum of the current and a finite number of previous values of the input.

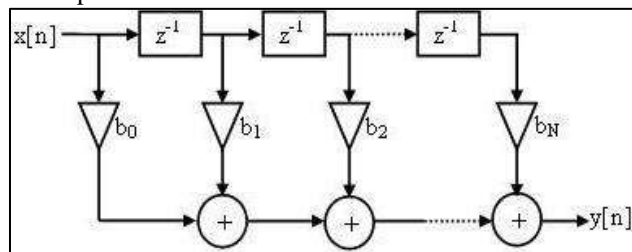


Fig. 2: Discrete-time FIR Filter

The operation is described by the following equation,

$$y[n] = b_0x[n] + b_1x[n - 1] + \dots + b_Nx[n - N] = \sum_{i=0}^N b_i x[n - i] \quad (1)$$

It shows that the output sequence $y[n]$ is the function of input sequence $x[n]$ and its delayed form and the coefficients. Here N is the order and b_i are the filter coefficients, also known as tap weights, that make up the impulse response. For DSP and real time

applications, filters with higher order should be employed it is due to the fact that higher the order sharper is the transition between the pass band and the adjacent stop band [10].

D. CIC Decimator

Fig 3 shows the structure of CIC decimator. It uses a comb stage followed by a down sampler and an integrator stage [2]. The building blocks of comb stage and integrater stage is shown in Fig 4.

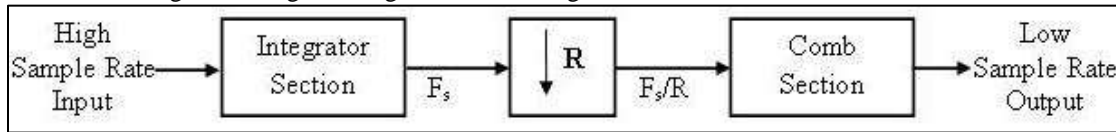
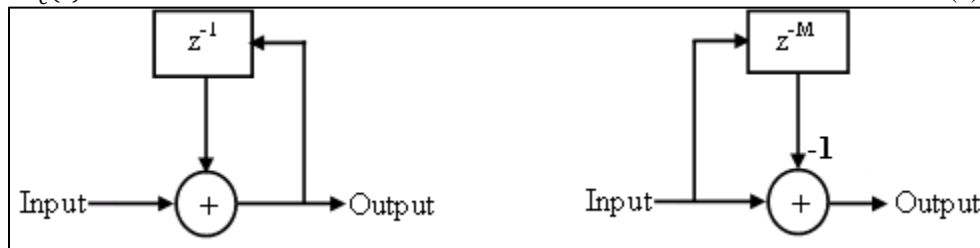


Fig. 3: Basic Block Diagram of CIC Decimator

The comb section is an FIR filter described by $y[n] = x[n] - x[n-RM]$, where M is the delay, and R is the up sampling factor. M can be any positive integer, but it is usually limited to 1 or 2. The corresponding transfer function of the comb section is given as,

$$H_c(z) = 1 - z^{-RM} \quad (2)$$



a) Simple Integrator Stage

b) Simple Comb Filter Stage

Fig. 4: Building Blocks of CIC Filter

The integrator section is a single-pole IIR filter with a unity feedback coefficient. The integrator is described by $y[n] = y[n-1] + x[n]$, where $y[n]$ is the output, $y[n-1]$ is previous value of output, and $x[n]$ is the input. This system is also known as an accumulator[4]. The transfer function for integrator is given by the following equation.

$$H_I(z) = \frac{1}{1-z^{-1}} \quad (3)$$

III. CDMA 2000, WCDMA SPECIFICATION AND THEIR DDC STRUCTURE

The details of CDMA 2000 and WCDMA, their specifications and their detailed DDC block Diagram for both application is discussed below.

A. CDMA-2000 (Code Division Multiple Access)

CDMA2000 (also known as C2K or IMT Multi Carrier (IMT-MC)) is a family of 3G mobile technology standards for sending voice, data, and signaling data between mobile phones and cell sites. It is developed by 3GPP2 as a backwards-compatible successor to second-generation CDMA One (IS-95) set of standards. The CDMA 2000 air interface standards specify a spread spectrum radio5 interface that uses Code Division Multiple Access (CDMA) technology to meet the requirements for 6 third generation (3G) wireless communication systems. CDMA2000 compares to UMTS, a competing set of 3G standards, which is developed by 3GPP and used in Europe, Japan, and China.

B. WCDMA (Wideband Code Division Multiple Access)

WCDMA is a spread-spectrum modulation technique, that is, one which uses channels whose bandwidth is much greater than that of the data to be transferred. Instead of each connection being granted a dedicated frequency band just wide enough to accommodate its envisaged maximum data rate, WCDMA channels share a much larger band. The demodulation technique encodes each channel in such a way that a decoder, knowing the code, can pick out the wanted signal from other signals using the same band, which simply appear as so much noise. The design parameters are given in Table 1 [14].

Table – 1

Design parameters of WCDMA and CDMA 2000

Parameter	WCDMA	CDMA 2000
Carrier Bandwidth	5 MHz	1.25 MHz
Number of Carrier	1	1
Baseband chip rate	3.84 MCPS	1.2288MCPS
IF sample rate	61.44 MSP 16x3.84 MSPS	61.44 MSPS 50x1.2288 MSPS
Transmit spectral mask	Upto 70 dB	Upto 70 dB

C. DDC Structure for WCDMA Application

The DDC structure for WCDMA is shown in Fig 5.[15]. The input signal for the digital down converter of WCDMA is the up sampled signal at the frequency 61.44 MHz. The required output frequency (i.e.) the original frequency is 3.84 MHz. This means the up sampled signal must undergo 16 levels of down conversion to get back the original signal. It has three stages of down conversion. In the first stage, the input signal is down converted by a factor of 2 and passed into a low pass FIR decimator.

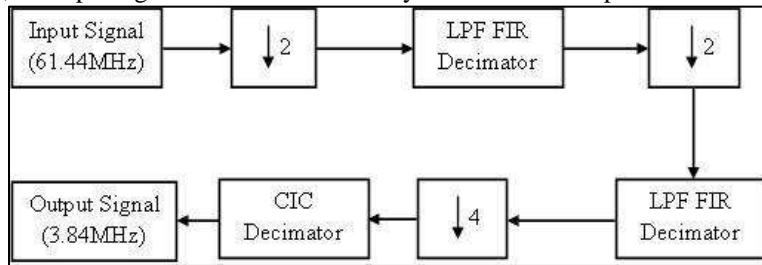


Fig. 5: DDC Structure for WCDMA

In the second stage, the signal is again down converted by a factor of 2 followed by a low pass FIR decimator. In the final stage, the signal is down converted by a factor of 4 and then passed into CIC decimator and the signal at frequency 3.84 MHz is obtained. Fig 5 shows the DDC structure for WCDMA[15].

D. DDC for CDMA2000 Application

The input signal for the digital down converter of CDMA 2000 is the up sampled signal at the frequency 61.44 MHz[12]. The required output frequency (i.e.) the original frequency is 1.2288 MHz. This means the up sampled signal must undergo 50 levels of down conversion to get back the original signal. It has three stages of down conversion. In the first stage, the input signal is down converted by a factor of 2 and passed into a low pass FIR decimator. In the second stage, the signal is again down converted by a factor of 5 followed by a low pass FIR decimator. In the final stage, the signal is down converted by a factor of 5 and then passed into CIC decimator and the signal at frequency 1.2288 MHz is obtained. Fig 6 shows the DDC structure for CDMA 2000.

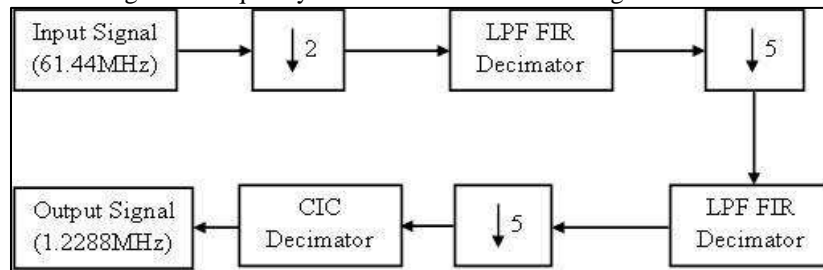


Fig. 6: DDC Structure for CDMA 2000

IV. PROPOSED SHIFT & MUX BASED MULTIPLIER

Since the DDC comprises of FIR filters of higher order an efficient multiplier is required to reduce the complexities. The SHIFT and MUX based multiplier is proposed in our design implementations which has less complexities than conventional DA and LUT based multipliers [11]. To understand the generation of partial products in SHIFT and MUX based multiplier, let the multiplier be x and multiplicand be c . Now, if the bit in multiplier x is 0, then the corresponding partial product is zero. If the bit is 1, the multiplicand undergoes shifting to get the partial product. The bit of multiplicand at n th position will be shifted n times, that is, zeroth bit will be shifted zero times, first bit will be shifted one time and so on, and the end bit must be extended in each partial products. The most significant bit (MSB) of multiplier is the sign bit. Apart from shifting, MSB is 2's complemented before being added with other partial products, adding all the partial products finally gives the multiplication product. The Fig 7 shows the proposed multiplier architecture and Fig 8 depicts how the multiplier works.

Table – 2

Operation of SHIFT & MUX based Multiplier

X	X in terms of power 2	OUTPUT
0000	0	(0)C
0001	2^0	(1)C
0010	2^1	(2)C
0011	$2^1 + 2^0$	(3)C
0100	2^2	(4)C
0101	$2^2 + 2^0$	(5)C
0110	$2^2 + 2^1$	(6)C
0111	$2^2 + 2^1 + 2^0$	(7)C

1000	-2^3	$(-8)C$
1001	-2^3+2^0	$(-7)C$
1010	-2^3+2^1	$(-6)C$
1011	$-2^3+2^1+2^0$	$(-5)C$
1100	-2^3+2^2	$(-4)C$
1101	$-2^3+2^2+2^0$	$(-3)C$
1110	$-2^3+2^2+2^1$	$(-2)C$
1111	$-2^3+2^2+2^1+2^0$	$(-1)C$

In the Table 2, when MSB is 0 there is no 2's complement form required. If MSB is 1, it has to be considered as -8, and other bits are added to it. For example, 1111 is calculated as $-8+4+2+1=-1$. Thus it gives the 2's complement form of it.

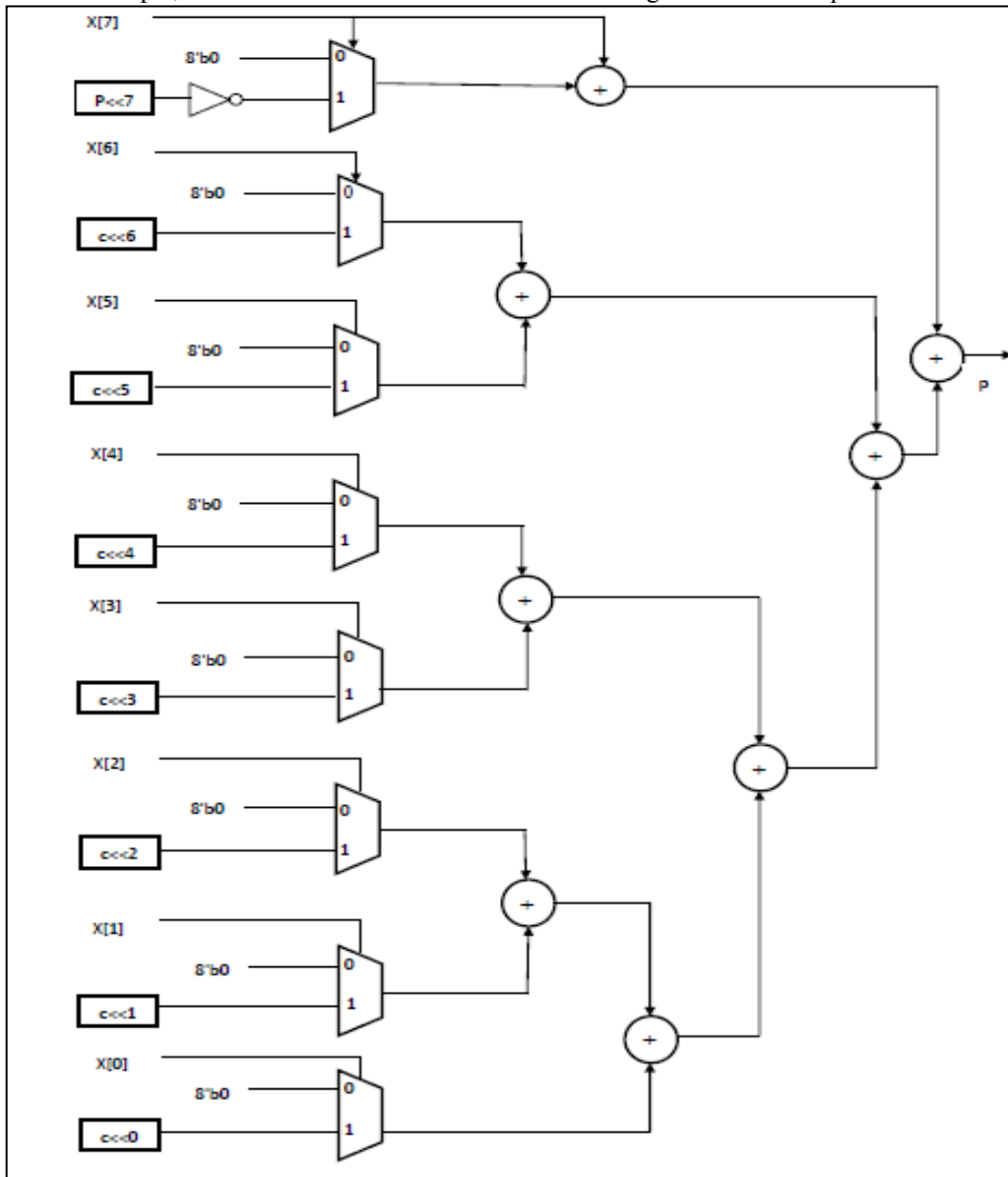


Fig. 7: Architecture of SHIFT & MUX based Multiplier

V. SYSTEM IMPLEMENTATION, RESULTS & DISCUSSION

This section discusses about two implementation methods and simulation results for both WCDMA and CDMA 2000. The performance comparison between two methods for both application is discussed.

A. Simulink Model & Results of WCDMA DDC

Fig 8 shows the Simulink model of WCDMA DDC. The source is given as the sine wave input which is followed by first level of down sampler followed by first level Lowpass FIR decimation filter followed by second down sampler and second Lowpass FIR decimation filter followed by last CIC filter with integrator and comb stages with final downsampler[14].

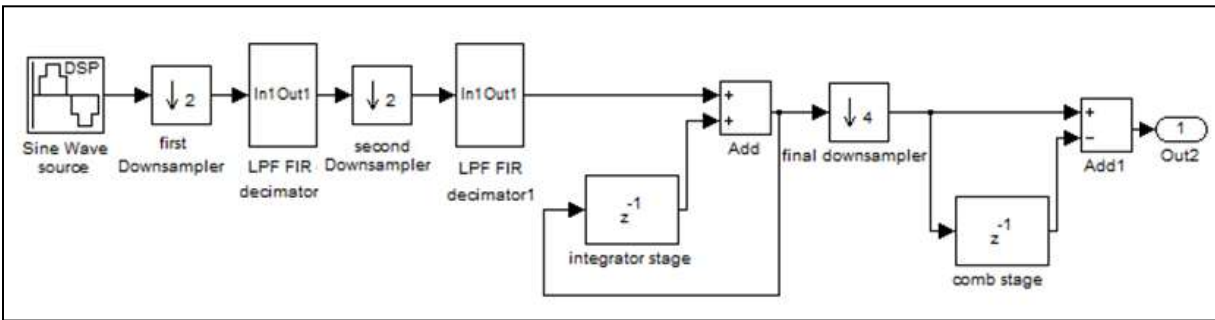


Fig. 8: Simulink Model for WCDMA DDC

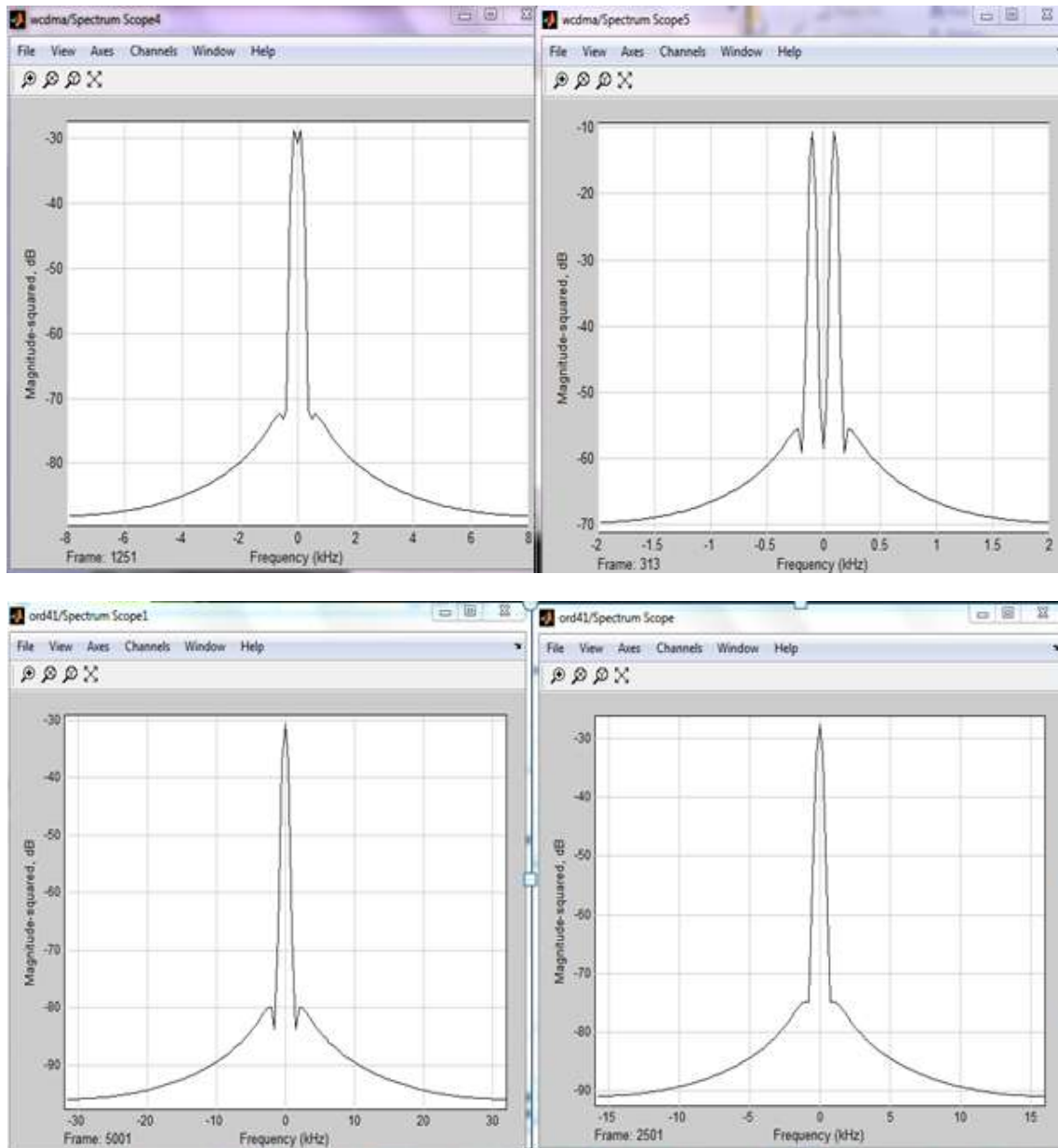


Fig. 9: Simulink Output of WCDMA DDC

The frequency response of this model is shown in Fig 9. The first frequency versus magnitude plot is the input and it is in the frequency range from -30 to +30 kHz which is reduced to range from -15 to +15 kHz when down sampled by factor 2 shown in plot 2 and further reduced to range from -8 to +8 kHz when down sampled again by factor 2 shown in plot 3 and in the final plot the frequency almost comes in the range of -2 to +2 kHz. This shows the the input is downsampled by a factor of 16 and hence the input signal frequency will be reduced from frequency range of 61.44 to 3.84 MHz [12].

B. WCDMA DDC Designed with SHIFT & MUX based Multiplier

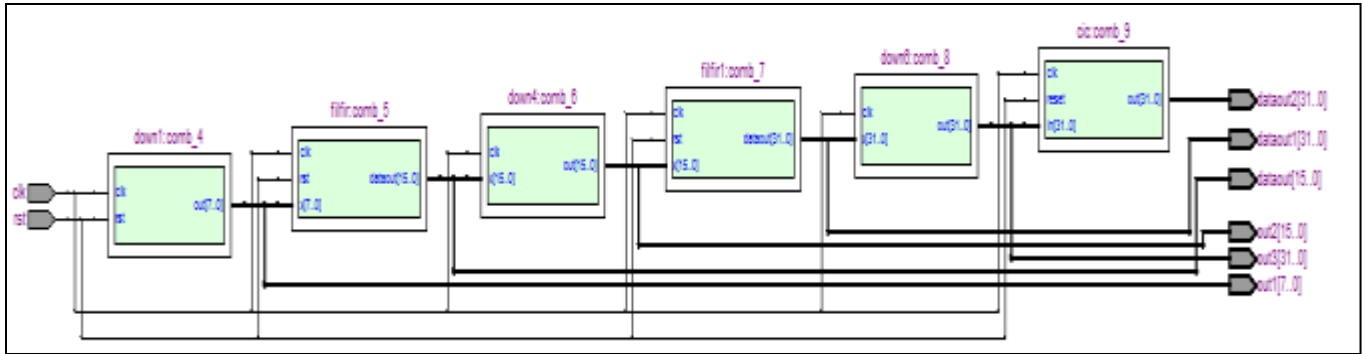


Fig. 10: RTL View of WCDMA DDC Designed with SHIFT and MUX based Multiplier

Fig 10 depicts the RTL view of WCDMA DDC designed with SHIFT and MUX based multiplier. In the WCDMA DDC Architecture the input is first down sampled by factor 2 and the output of it is given to first FIR lowpass decimator and the output of this is fed into the second downsampler where it is down sampled by factor 2 and is given to the second FIR lowpass decimator and the output is fed in to the last down sampler where it is down sampled by a factor 4 and finally given to the CIC decimator which results in the total down sampling factor of 16 and the frequency is reduced from 61.44 MHz to 3.84 MHz.

Fig 11 depicts the RTL view of SHIFT and MUX based multiplier. By using the SHIFT and MUX based multiplier in FIR filter designing process, the overhead is reduced to a large extent compared to other signed multipliers as the SHIFT and MUX based Multiplier gives the multiplied output in a single clock cycle. By storing the partial products in registers we can also implement pipelined processing.

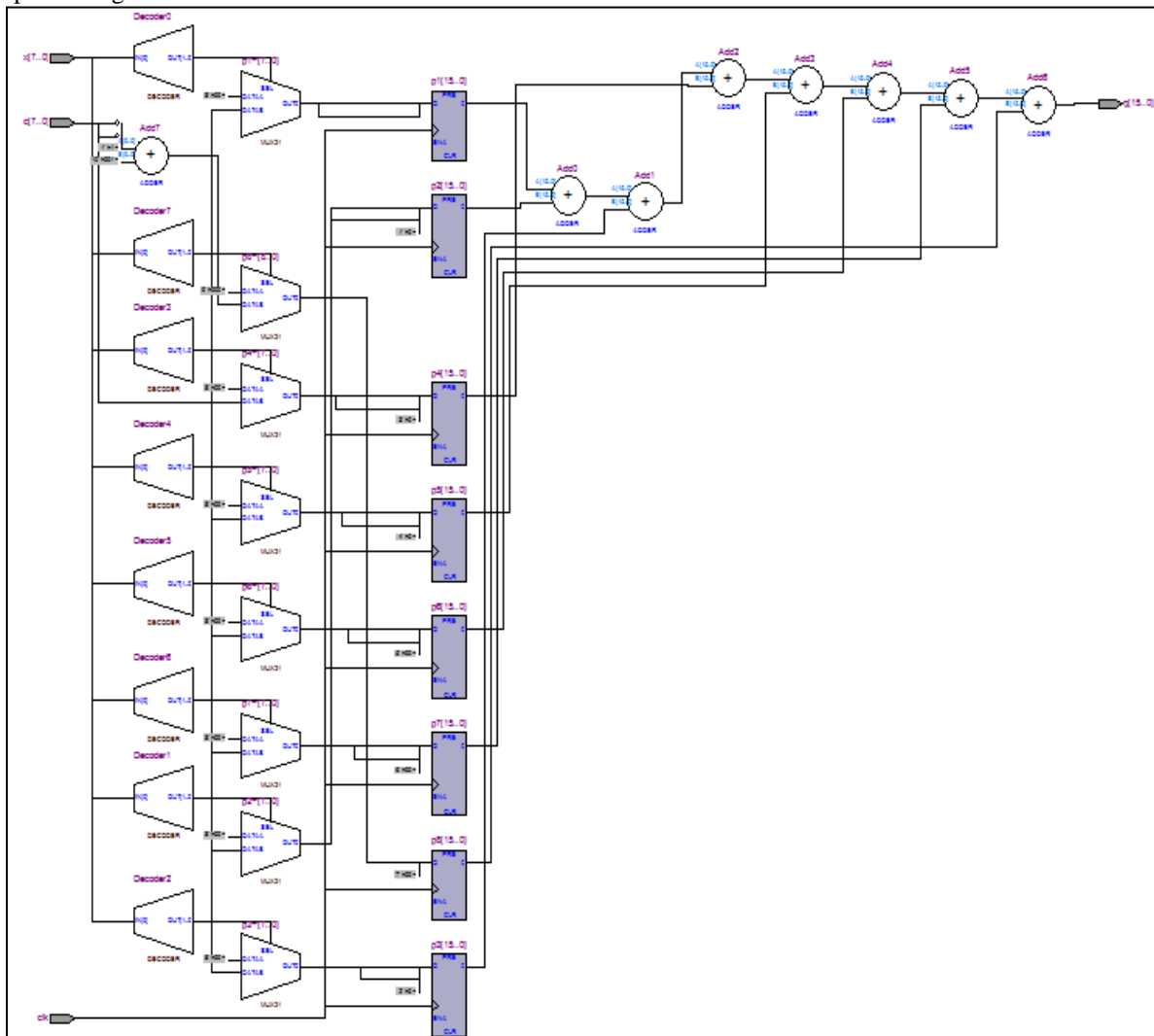


Fig. 11: RTL view of SHIFT and MUX based Multiplier

C. Simulink Model & Results of CDMA 2000 DDC

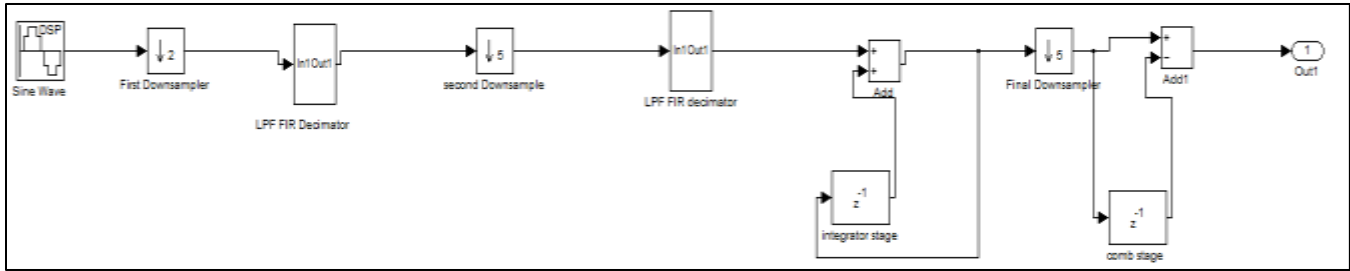


Fig. 12: Simulink Model of CDMA 2000 DDC

The source is given as the sine wave input which is followed by first level of down sampler followed by first level Lowpass FIR decimation filter followed by second down sampler and second Lowpass FIR decimation filter followed by last CIC filter with integrator and comb stages with final downsampler[14].

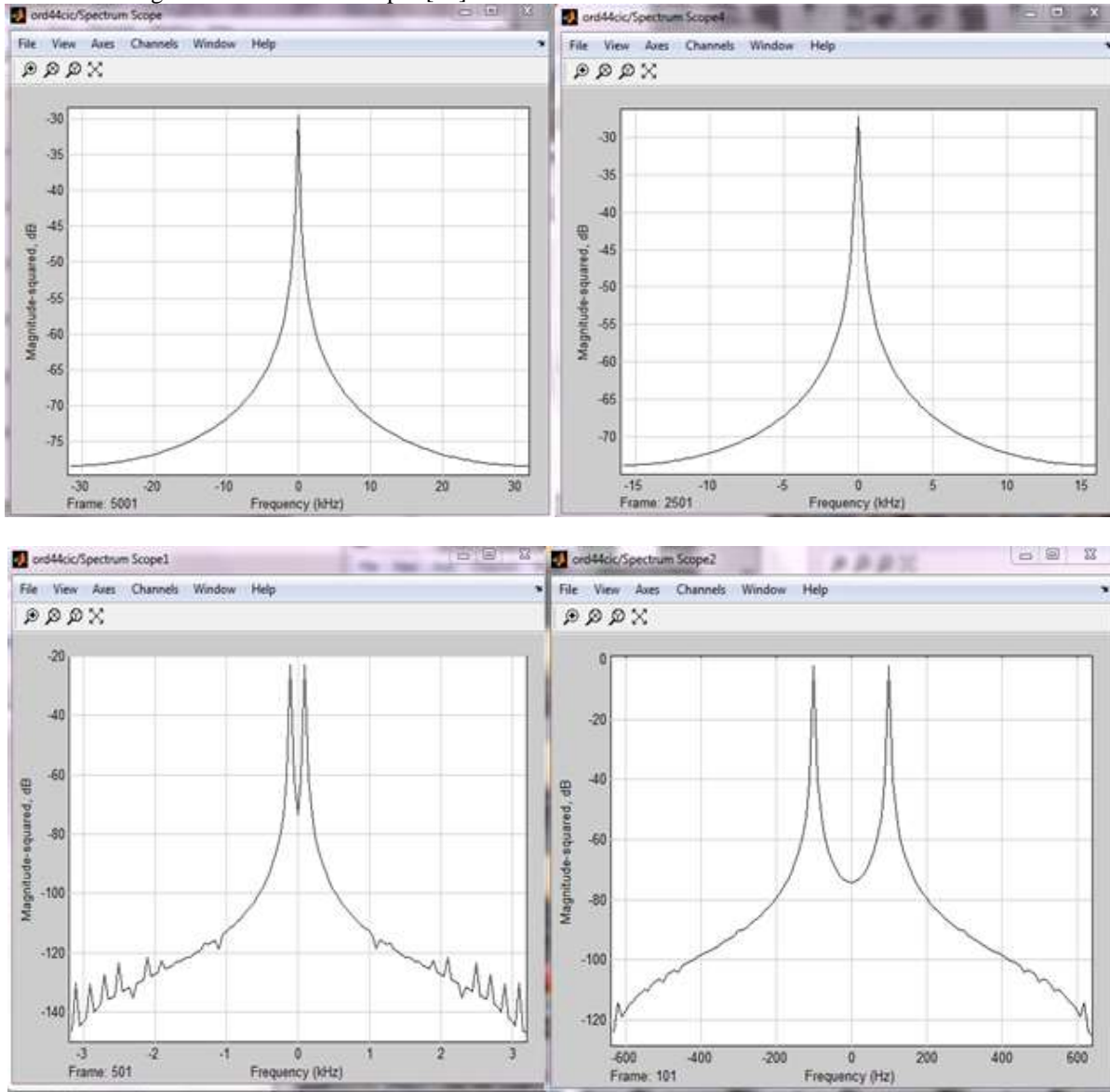


Fig. 13: Simulink Model Output for CDMA 2000 DDC

Fig 13. depicts the simulation result obtained at intermediate stage and at the output of DDC for CDMA 2000 using Simulink model. The first frequency versus magnitude plot is the input and it is in the frequency range from -30 to +30 kHz which is reduced to range from -15 to +15 kHz when down sampled by factor 2 shown in plot 2 and further reduced to range from -3 to +3 kHz when down sampled again by factor 5 shown in plot 3 and in the final plot the frequency almost comes in the range of -600 to

+600 Hz. This shows that the input is downsampled by a factor of 50 and hence the input signal frequency will be reduced from frequency range of 61.44 to 1.228 MHz.[12].

D. CDMA 2000 DDC Designed with SHIFT & MUX based Multiplier

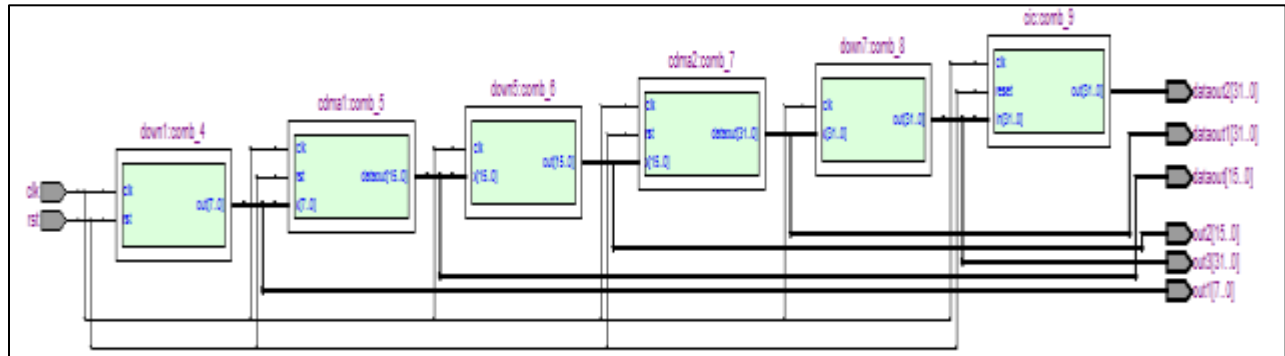


Fig. 14: RTL View of CDMA 2000 DDC Designed with SHIFT and MUX based Multiplier

The RTL view of CDMA 2000 DDC designed with SHIFT and MUX based multiplier is shown in Fig 14. In this CDMA 2000 DDC architecture the input is first down sampled by factor 2 and is given to first FIR RRC decimating filter and the output of this is fed into the second downsampler where it is down sampled by factor 5 and given to the second FIR RRC decimator and its output is fed into the last down sampler where it is down sampled by a factor 5 and finally given to the CIC decimator which results is the total down sampling factor of 50 and the frequency is reduced from 61.44 MHz to 1.228 MHz.

E. Performance Comparison between the DDC code Generated from Simulink Model & Verilog Code Written using SHIFT & MUX based Multiplier

The performance of the DDC designed using simulink as well as verilog code written using SHIFT and MUX based multiplier is analyzed by synthesizing the design on Altera Cyclone II EP2C35F672C6 FPGA device. The important parameters such as area occupied, maximum delay, and the power dissipation in both implementation is tabulated and analysed. Table 3. Shows the comparison of results for WCDMA DDC and Table 4. Shows the comparison of results for CDMA 2000 DDC.

Table – 3

Comparison of Results for WCDMA DDC

PARAMETERS	MATLAB GENERATED CODE	CODE WRITTEN IN VERILOG
Total logic elements	31,738/33,216	7295/33,216
Total registers	1411	2354
Total thermal power dissipation (mW)	126.27	118.07
Core static thermal power dissipation(mW)	79.95	79.98
I/O Thermal power dissipation(mW)	46.29	38.12
Worst case Tsu(ns)	84.10	3.338
Worst case Tco(ns)	93.65	68.61
Worst case Th(ns)	92.62	0.624

Table – 4

Comparison of Results for CDMA 2000 DDC

PARAMETERS	MATLAB GENERATED CODE	CODE WRITTEN IN VERILOG
Total logic elements	32,738/33,216	7202/33,216
Total registers	1418	2564
Total thermal power dissipation (mW)	126.27	126.33
Core static thermal power dissipation(mW)	79.95	79.98
I/O Thermal power dissipation(mW)	46.29	46.35
Worst case Tsu(ns)	84.10	4.377
Worst case Tco(ns)	93.65	68.319
Worst case Th(ns)	92.62	0.251

From the above comparison we can clearly visualize that the DDC codes developed using SHIFT and MUX based multiplier has very less area, power and time complexities compared to the DDC codes generated from simulink model. For example the total logic elements used is reduced from 31738 to 7295 for WCDMA DDC and is from 32738 to 7202 for CDMA 2000 DDC, results in an area reduction of 77.01% and 78% respectively. Similarly the reduction in maximum delay would give the speed improvement of 26.73% and 27.05% for WCDMA DDC and for CDMA 2000 DDC respectively. The power dissipation in the SHIFT and MUX based multiplier is either smaller or almost the same when compared to the implementation of MATLAB generated code. The increase in the number of registers is due to the use of a pipelined form of architecture in SHIFT and MUX based multiplier.

VI. CONCLUSION

This paper describes the importance of DDC in SDR and how the DDC for the two SDR applications WCDMA and CDMA 2000 have been implemented efficiently. The digital down converter for WCDMA and CDMA2000 specifications are designed and simulated in MATLAB simulink tool. Code generated using MATLAB is synthesized on Altera Cyclone II EP2C35F672C6 FPGA device. The DDC structure for both standards built again by redesigning it with SHIFT and MUX based multiplier, which is also synthesized on same FPGA device. The comparison between these two implementation shows that the SHIFT and MUX based multiplier structure provides improved performance in terms of area, delay and power, thus making the proposed design suitable for SDR application.

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