Low Power and High Speed Carry Select Adder using Skip Logic

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Abstract

This paper clearly focused on Carry Skip Adder (CSA) which gives an advantage of reducing delay, area and power. Usually Ripple carry adder which is used to perform arithmetic operations to perform fast design duration compared with other conventional methods, but lacks with a limitation of generating carry bits. The proposed architecture is designed using Verilog HDL and is then synthesized using Xilinx.

Keywords: Carry select adder (CSLA), Carry skip adder (CSA), delay, power consumption

I. INTRODUCTION

In logic circuitry and digital electronic circuits, adder is an inevitable and important component. It is the main area or research in VLSI field system design for improving the performance, participation and output of a digital system. The performance depends on area, power consumption and delay. The participation depends upon sub carriers we use. The output depends upon the circuit function. Adders are not only applicable in arithmetic operations, but also for calculating addresses, table indices, increment and decrement operators, and similar operations.

In basic, an adder is a digital circuit that performs addition of numbers. In many computer systems and kind of processors adders are used in the ALU. Most of the common adders operate on binary numbers. Generally adders use the combinations of logic gates to combine binary values for calculating the sum. The adders are grouped based upon their aptness to accept and amalgamate the digits. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an adder is generated sequentially only when the previous bit position is has been summed and a carry propagated into the next position is obtained.

The Carry select adder is implemented in wide range of mathematical systems to moderate the problem of carry propagation delay by selecting a carry to generate a sum. However, the carry select adder is not speed efficient because it uses pairs of ripple carry adders to generate the partial sum and carry by taking carry input into the account, the final sum and carry are selected by the multiplexers. Relating carry skip adder and ripple carry adder the best adder is carry skip adder because the delay path is finer and lower. So, the ripple carry adders are modified into carry skip adder to improve the speed of addition in carry select adder.

A. Ripple Carry Adder

A ripple carry adder is a logic circuit in which the carry- out of each full adder is the carry of subsequent next most consequential full adder. The reason behind the purpose of RCA is for addition of two N- bit numbers. It composes of N- digits numbers. From the proceeding full adder block, carry output of its presumptuous full adder. This form of distinctive adders is called as Ripple Carry Adders. It is so called because carry ripples to next full adder. The paramount muddle for binary addition using RCA is the carry chain. Proliferating the input operand width increases the carry chain length. The subjugate instance transpire when the carry progress the elongated feasible esplanade initiating the Least Significant Bit (LSB) to the Most Significant Bit (MSB). In order to dwindle the delay in RCA (or) to promulgate the carry in prosper, the carry look ahead adder. Inherently this avatar of adder toil on two operations called promulgates and trigger. Proliferating the adder bit width increases the carry entanglement.

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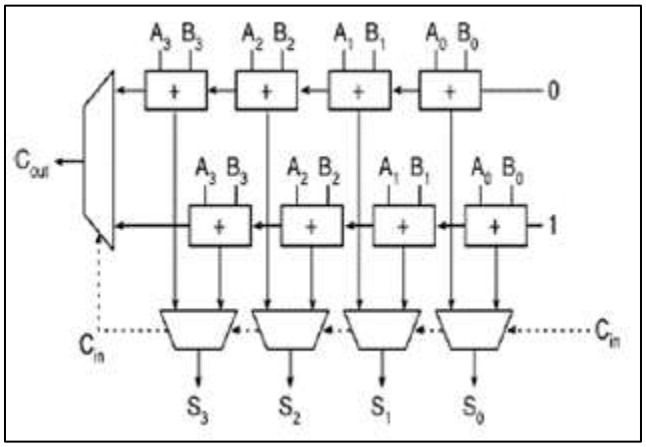
B. Multiplexer

Multiplexer (or mux) is a device that selects multiple input signals and forwards the input into a single line. A multiplexer has n selection lines, which are used to select which input line to send to the output. Multiplexers are used to increase the data flow over network with certain amount of time and bandwidth. It is also called as data selector. Multiplexers can also be used to operate Boolean functions of multiple variables.

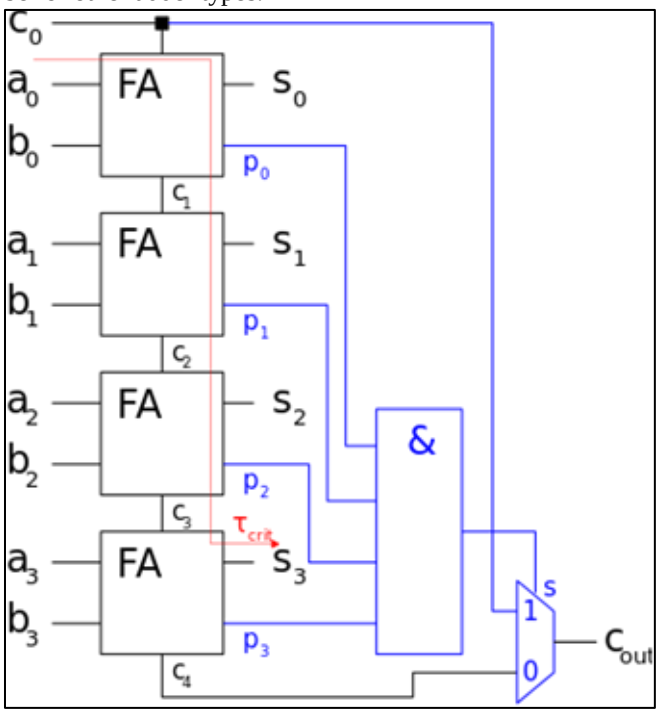
C. Carry Select Adder

The carry select adder generally consists of two RCA and one mux. The 2 n-bit numbers are summed upon using the two adders, it is performed with the assumption of carry as 0 & 1 and the results are calculated twice. The appropriate carry is selected with a multiplier and is controlled by the carry from previous adders. The carry select adder is simpler and faster one, having a gate level depth of 0(√n). In total, the carry propagation time through an n-bit adder block is reduced from O(n) to the number of stages times the delay of the multiplexers.



D. Carry Skip Adder

A Carry Skip Adder is implemented to improve the delay of ripple carry adder when compared with other adders. A Carry skip adder is also known as Carry-bypass adder. The carry skip adder comes from a by-pass adder and it uses a ripple carry adder for an adder implementation. The formation of carry skip adder block is realized by improving worst case delay. This adder is proficient one in terms of area usage and power consumption. The carry skip optimization problem for variable block sizes and multiple levels for an arbitrary device process node was solved by Thomas W. lynch. This reference also shows the carry skip adder is same as parallel prefix adder and is thus related to and for sum configurations identical to the han Carlson, the brent-kung. The Kogge stone adder and a number of other adder types.



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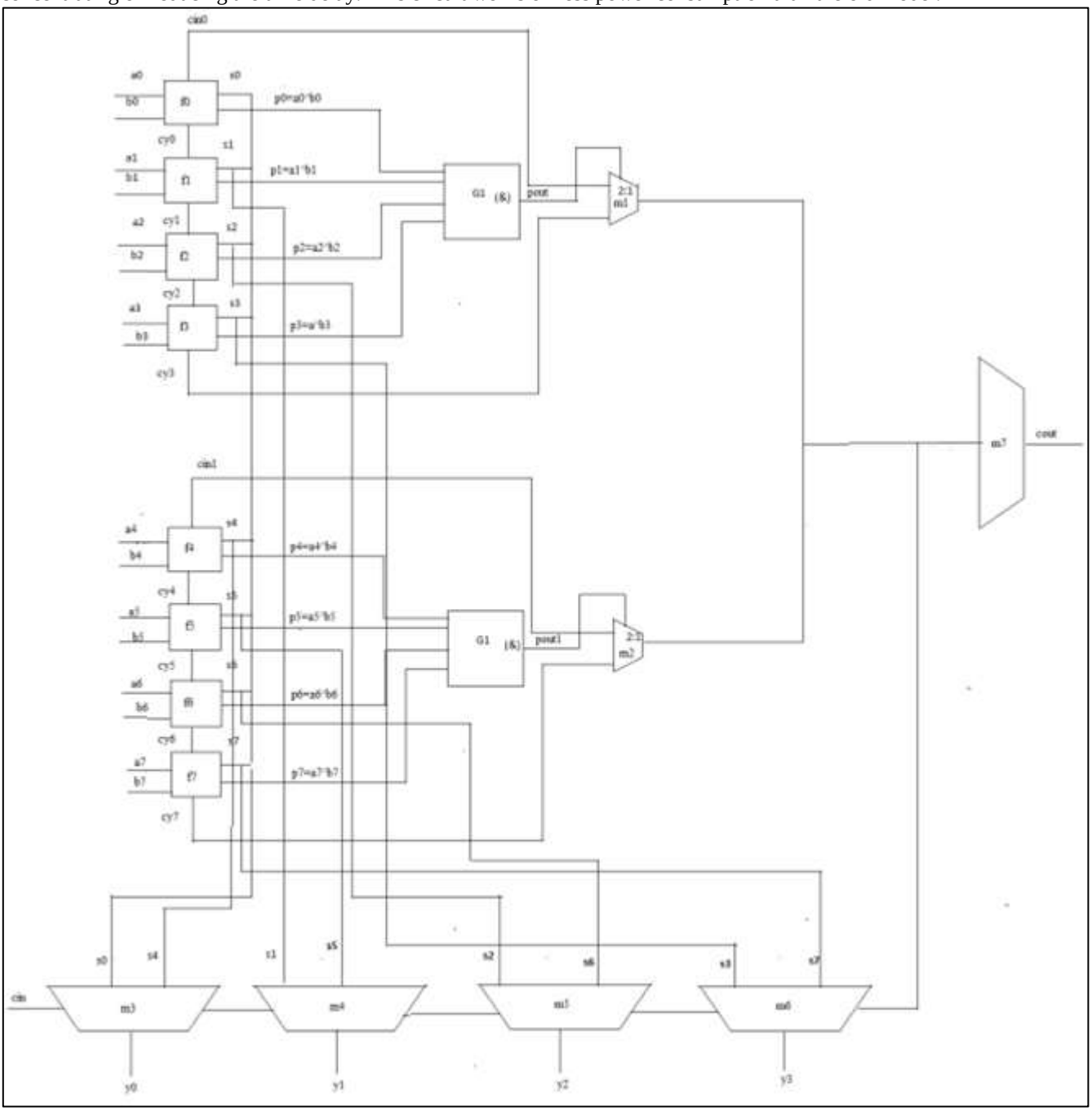
E. Proposed Thesis

We have proposed logic to implement the carry select adder using carry skip adder instead of full adder. Two 4-bit carry skip adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Then series of multiplexers are used and then finally the carry and sum is generated. The purpose of the designers innovation from the existing models is concentrating on reducing the time delay. This circuit works on less power consumption than the old model.



F. Xilinx Tool

Xilinx ISE (Integrated synthesis environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate a design reaction to different stimuli and configure the target device with the programmer. It is a design environment for FPGA and is tightly coupled to the architecture of such chips and cannot be used with FPGA products from other vendors. The primary user interface of the ISE is the project navigator, which includes the design hierarchy, a source code editor, an output console and processes tree. The design hierarchy consists of design modules which dependencies are interpreted by the ISE and displayed as a tree structure

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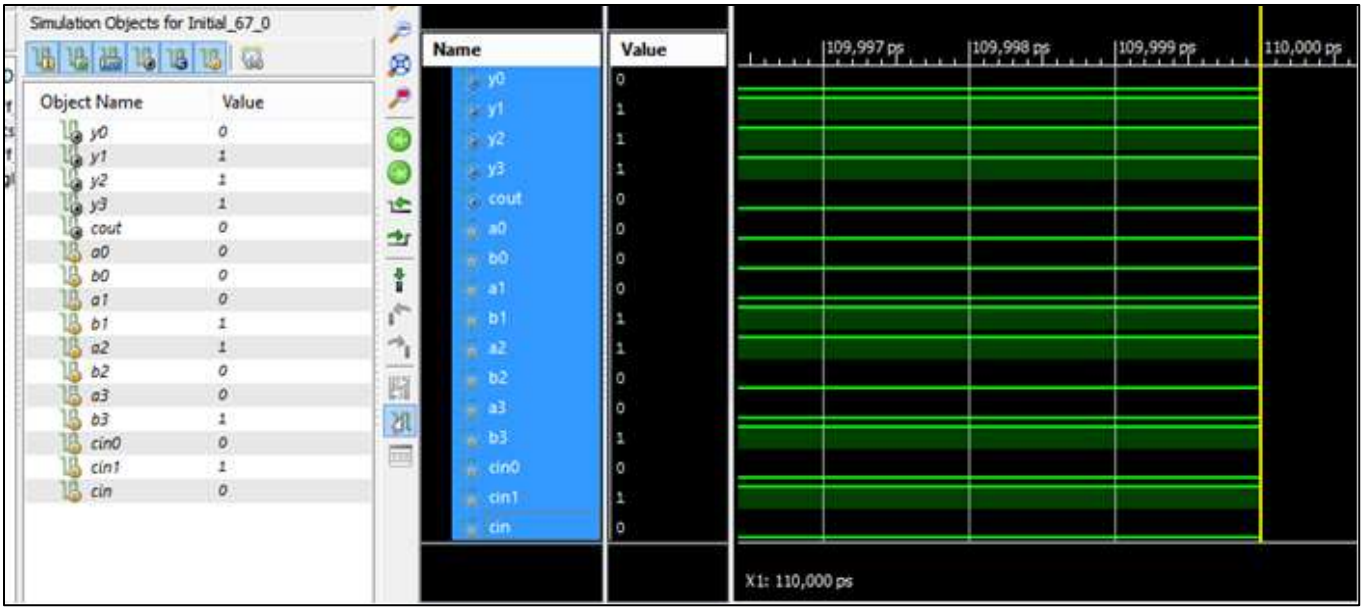
II. RESULT ANALYSIS

A. Simulation Result



B. Power Analysis

Name	Power (W)	Used	Total Available	Utilization (%)
Logic	0.000	6	4896	0.1
Signals	0.000	15	---	---
IOs	0.000	16	158	10.1
Total Quiescent Power	**0.052**			
Total Dynamic Power	**0.000**			
Total Power	**0.052**			

C. Device Utilization Summary

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Device utilization summary:
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Selected Device : 3s250epq208-4

 Number of Slices:                        3  out of   2448     0%
 Number of 4 input LUTs:                  5  out of   4896     0%
 Number of IOs:                          16
 Number of bonded IOBs:                  16  out of    158    10%

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D. Timing Report

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=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
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Speed Grade: -4

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 8.972ns
```

III. CONCLUSION

The implementation of carry select adder using Ripple carry adder has been formatted for the same desired output. The blocks of RCA is replaced by the blocks of carry skip adder. The skip logic is used by the designer to skip the time delay as the carry is carried at the last. This has been formulated for time sake if the circuit. This makes the circuit work quickly and the output is obtained fast.

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