Power Efficient Carry Skip Adder Based on Static 125nm CMOS Technology

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Abstract

In a digital circuit theory, combinational logic is a type of digital logic implemented by Boolean circuits, where the output is pure function of the present input. A carry skip adder which is also known as carry by pass adder is an adder implementation that improves on the delay of a ripple carry adder with little effort compared to other adders, In which, it have the low power consumption, a high degree of regularity and simplicity that the carry ripple chain is connected to n-input AND gate. The resulting bit is used as the select bit a multiplexer that switches either the last carry bit or the carry-in to the carry-out signal. The behaviour of the efficient Carry Skip Adder is designed using tanner eda tools which was useful and the currently existing carry skip adder is designed using xilnx software and lastly the layout for this research is designed with the help of multisim. With help of this research many newly created circuits can designed much smaller.

Keywords: Carry Skip Adder, CMOS, Static CMOS, 125nm, Tanner, Multisim, Xilinx, Half Adder, Full Adder, Ripple Carry Adder

I. INTRODUCTION

Adders play a major role in combinational circuits. A combinational circuit is said to be a circuit in which the output is depend upon the function given by the input which is implemented by various Boolean expression according to the connection given to each gate, though this may be considered controversial such as half adder, full adder, half subtractor, full subtractor, multiplexer, demultiplexer, encoder and decoder are also shared its classification under combinational logic. Carry skip adder consists of a simple ripple carry adder with speed up chain called skip chain the chain defines the distribution of ripple carry blocks if the carry is propagated at all position in the block then the carry signal entering into the block can directly bypass the carry skip adder optimization problem for variable block size and multiple levels for an arbitrary device process node was solved. A carry skip adders is also considered to be carry bypass adder, it is an adder implementation that improves on the delay of a ripple carry adder with little effort compared to other adders. This research paper is for designing a carry skip adder in 125nm static technology.

II. EXISTING SYSTEM

A full adder proceeds two binary numbers plus a carry or overflow bit. The output is a sum and carry bit. Full adders are generally linked to each other to append bits to an arbitrary length of bits such as 32 or 64 bit. A full adder is competently two half adders an ‘XOR’ and an ‘AND’ gate connected by an ‘OR’ gate. Half adder is a digital circuit that executes summation of numbers. The half adders adds two binary digits called as augend and addend and bring forth two outputs as sum and carry , ‘XOR’ is appertained to both input to produce sum and ‘AND’ gate is appertained to both inputs to produce carry . A Half Adder is made up of multiple gates which performs very basic operations according to the connections made in the CMOS (Complementary Metal Oxide Semiconductor

Gates used in the Carry Skip Adder are ‘xor’ gate, ‘and’ gate, ‘not’ gate. Generally gate are the building blocks of the combinational circuits .Gates are built using several numbers of transistor. We know that Moore’s law which states every six months number of the transistors used in a particular integrated circuit will be increased due to the technology enhancement. The XOR gate is a combinational logic gate that gives a ‘1’ output when the number of ‘1’ inputs is odd. An XOR gate implements an

exclusive or, that is, a '1' output results if one, and only one, of the inputs to the gate is '1'. If both inputs are '0' or both are '1', a '0' output results. In 'and' gate ,only multiplication operation can be done if the both input are same the output will be the same as the input and if the inputs are different then the output will '0'. In 'not' gate, contains only one input and the output is the output of the input if the input is '1' then the output will be '0' vice versa.

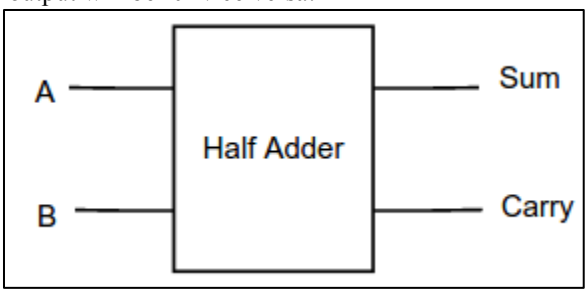


Fig. 1.1: Block diagram of Half Adder:

In fig 1.1 we can analyze that a half Adder consist of two inputs 'a' and 'b' and output 'sum'and 'carry'. Carry Skip Adder is buildup of multiple full adders and full adders are made with two half adder A truth table is a logically based mathematical table that expatiates the conceivable sequels of scenario the truth table suppresses the truth values thar would appear under the premises of the given scenario. The rows of a basic truth table contain the Boolean logic true or false values while the columns list the premises of a scenario as well as conclusion.

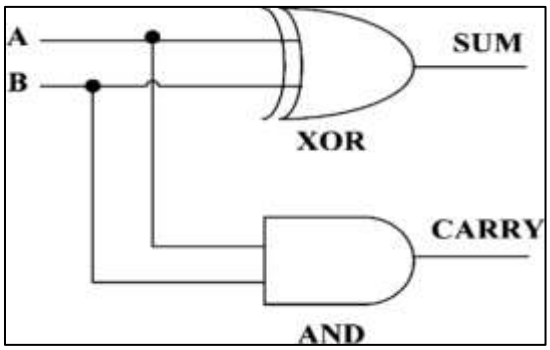


Fig. 1.2: Logic diagram of Half Adder:

In fig 1.2 Gates like 'xor', 'not', and 'and' Gates which are used to process the inputs and give the output. Each gate has a difference type of process algorithm based the connection given to the CMOS. The Boolean expression of the half Adder is as follows

SUM = ab' + ba'
CARRY= a . b

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Fig. 1.3: Truth Table of Half Adder:

In Fig 1.3 is a truth table of the half Adder which portrays the output of that logical circuit. A half Adder is a basic arithmetic processor which perform only subtraction its only function is to deduce a single bit binary from the input

III. CARRY SKIP ADDER

Carry skip adder consists of a simple ripple carry adder with speed up chain called skip chain the chain defines the distribution of ripple carry blocks if the carry is propagated at all position in the block then the carry signal entering into the block can directly bypass the carry skip adder optimization problem for variable block size and multiple levels for an arbitrary device process node was solved. A carry skip adders is also considered to be carry bypass adder.

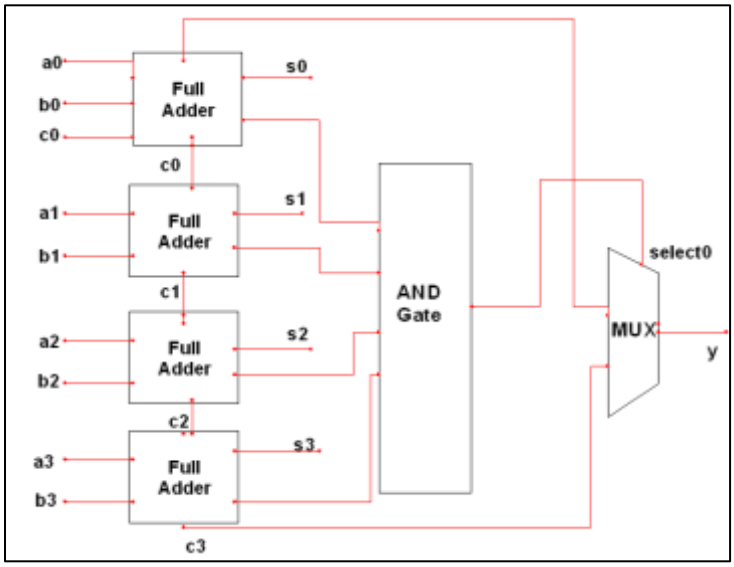


Fig. 2.1: Block diagram of Carry Skip Adder

In Fig2.1 we can analyze that a Carry Skip Adder consist of two inputs ‘a0’, ‘b0’, ‘c0’, ‘a1’, ‘b1’, ‘a2’, ‘b2’, ‘a3’ and ‘b3 whereas output ‘sum’and ‘carry’

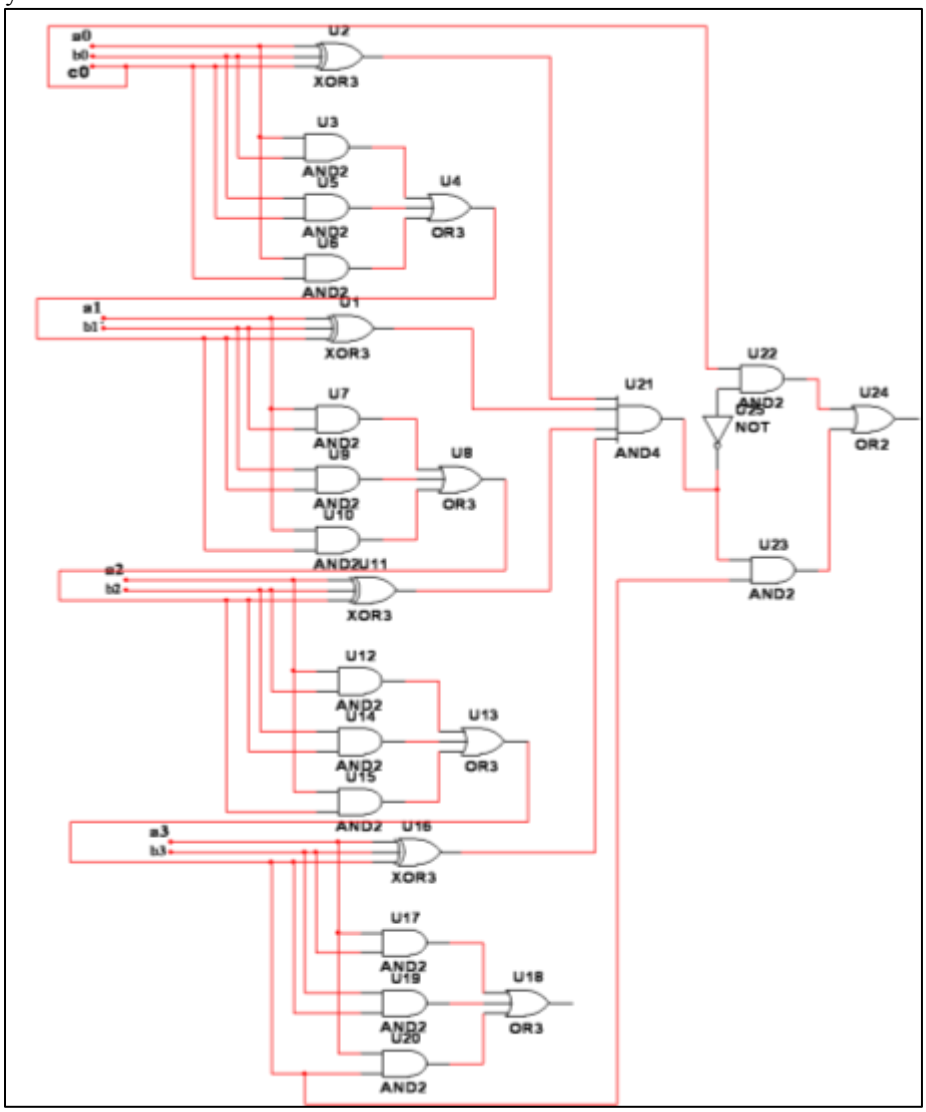


Fig. 2.2: Logic Diagram of Carry Skip Adder

In Fig 2.2 When the inputs are given through the respective labels gates present the circuits will process the data and perform the arithmetic operation subtraction and produce the Respective output sum and carry

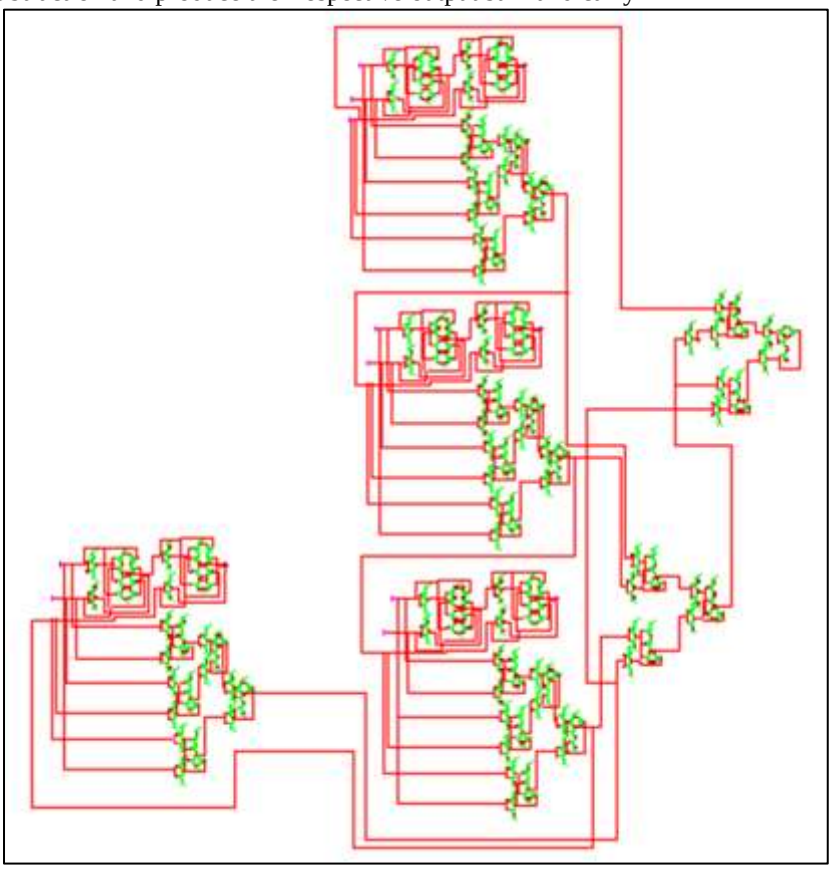


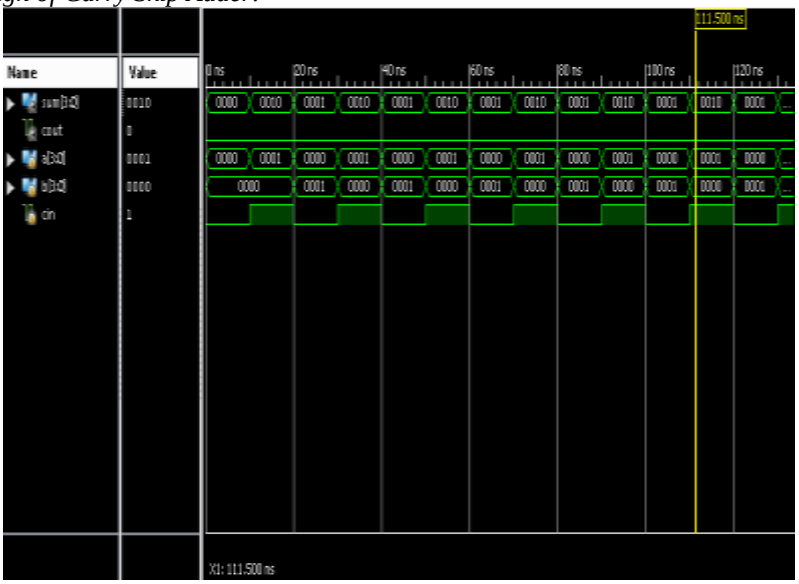
Fig. 2.3: CMOS Design o Carry Skip

In Fig 2.3The above Carry Skip Adder is designed using static cmos algorithm under 125 nm which is quite efficient and the results are same as the currently existing one When the inputs are given through the respective labels gates present the circuits will process the data and perform the arithmetic operation subtraction and produce the Respective output sum and carry

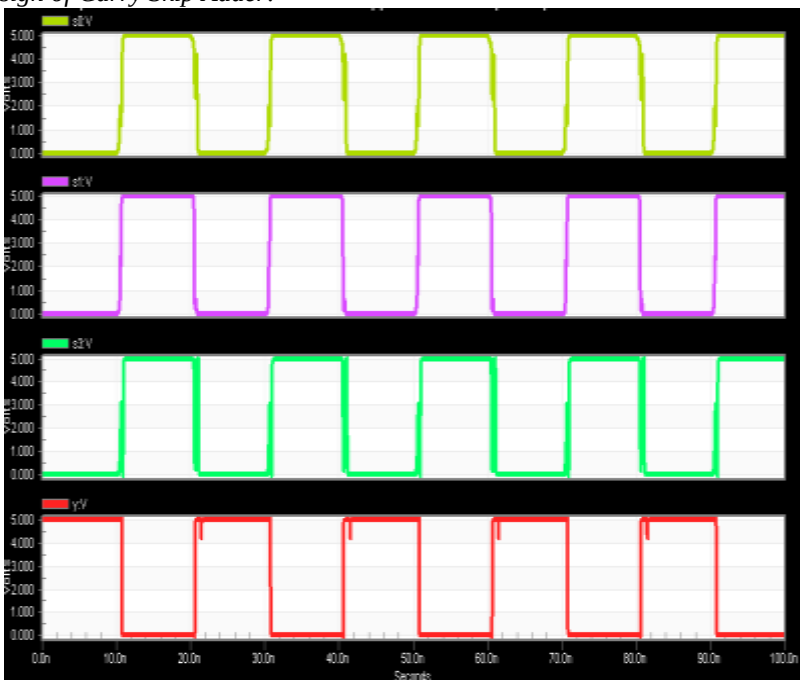
IV. RESULTS

A. Output

1) Waveform of Logic design of Carry Skip Adder:



2) *Waveform of CMOS design of Carry Skip Adder:*



V. CONCLUSION

It has been observed from the simulation results that performance of adder architectures varies with various CMOS design. The output of these two designs of Carry Skip Adder are same. The current fabrication size of Carry Skip adder is 125nm.If the fabrication size reduced to less than 100nm, the adder performance varies and can be absorbed using static (CMOS) technology. From this research the (CMOS) can be achieved by operating point within 0.9v.This research is very useful and more advantageous in future microprocessor industries.

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