Analogy Between Tri-Gate Transistor & Planar Transistor

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Abstract— Transistors are well known solid state device, invented in 1948 by John Bardeen and his team at Bell Laboratory which almost replaced the electron tubes. These transistors are current controlled devices which are capable of amplification. A Tri-Gate Transistor is a 3-D transistor with gate wraps around the channel from source to drain, as to the traditional 2-d planar design. Tri-entryway transistor assumes a basic part in vitality effective execution abilities since they offer impressively bring down leakage and expend substantially less power than today's planar transistors. A Tri-Gate transistor creation is determinedly used by Intel Corporation for the nonplanar transistor designing in Ivy Bridge and Haswell processors. This leap forward by Intel Corporation intensifies the upside of multi-door transistor with low viewpoint proportion channel. The paper clarifies relationship between different transistor to Tri-Gate Transistor.

Key words: Tri-Gate, Planar Transistor, Ivy Bridge, Intel Corporations,

I. INTRODUCTION

Transistors are well known solid state device, invented in 1948 by John Bardeen and his team at Bell Laboratory which almost replaced the electron tubes. These transistors are current controlled devices which are capable of amplification. A Tri-Gate Transistor is a 3-D transistor with gate wraps around the channel from source to drain, as to the traditional 2-d planar design. Three gates of this transistor wraps around the channel from source to drain, as to the traditional 2-d planar design. Thus, Tri-Gate Transistor is an innovation of semiconductor industry by the revolution of planar transistor into 3-dimensional one. A Tri-Gate transistor fabrication is firmly used by Intel Corporation in Ivy Bridge and Haswell processors. Planar (or flat) transistors were conceived in late 1950s what's more, have been the fundamental building piece of chips following the beginning of semiconductor industry. As semiconductor innovation moves more profound into the domain of nanotechnology (measurement littler than 100nm), where some transistor components might comprises of just a couple layer of molecules, is currently being composed in three measurements for enhanced execution and force qualities. Three gates likewise permit improved current in the "on" state, otherwise called drive current. These favourable circumstances mean lower power utilization and improved gadget execution.

This design of the device amplifies the advantage of multigate transistor over planer MOSFET with low aspect ratio channel. As Tri-Gate transistor is a 3-d structure, hence it also acquires following beneficial features against traditional one –

- Runs faster with better performance.
- Capsulated size.
- Low power dissipation and Increases battery life of devices

Intel, coming out on top in delivering high volumes of ever littler chip geometries, has made an approach to utilize these 3-d, or tri-gate transistors working together with other key semiconductors advancements to empower another time of vitality productive execution.

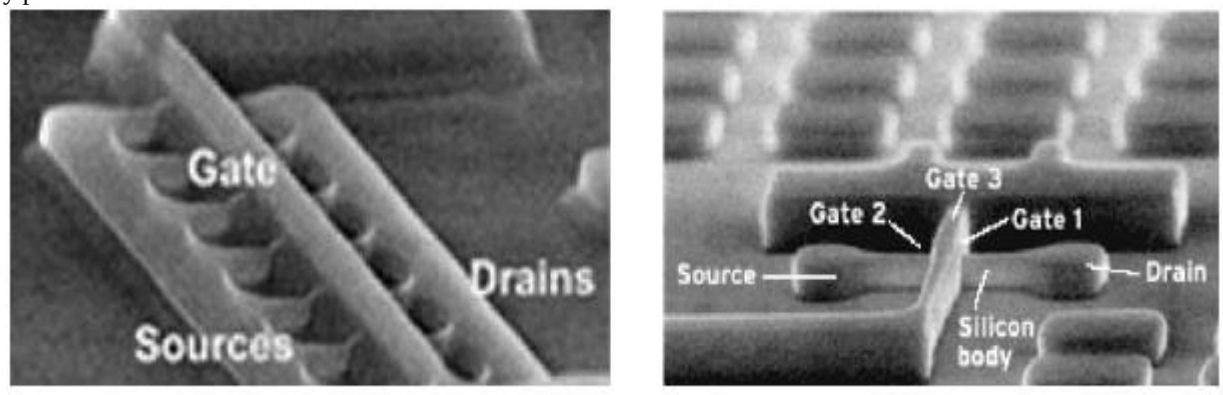

Fig. 1: Intel's Tri-Gate Transistors to enable 22nm Processors

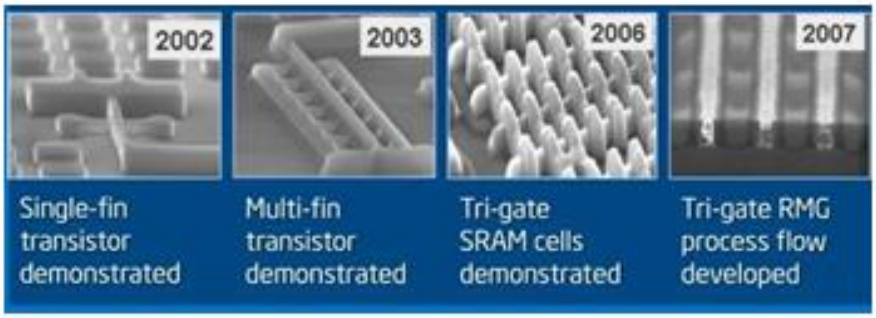

Fig. 2: Tri-Gate Achievement Results by Intel

II. ARCHITECTURE DESIGNING OF TRI-GATE TRANSISTOR

The Architectural design of Tri-Gate Transistor consists of three gates wrapped around the channel from source to drain, as to the traditional 2-d planar design. The three gates of transistor cover three out of four sides as shown in fig. 3.

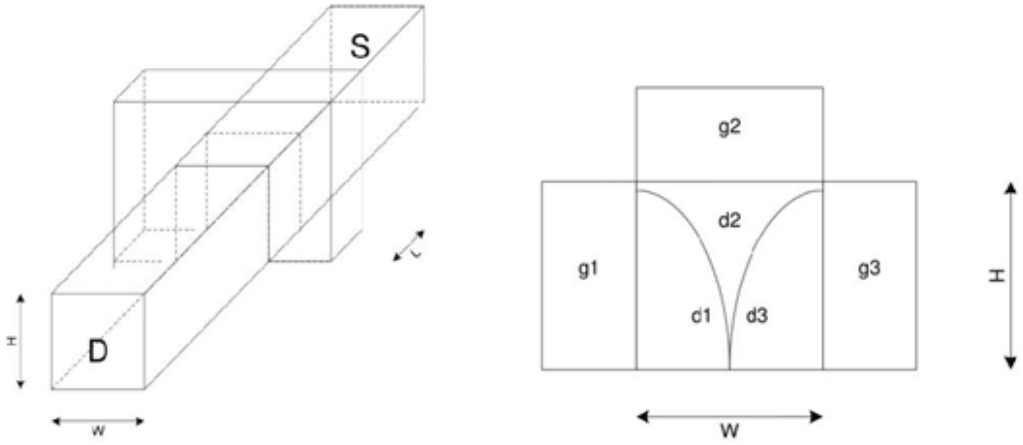

Fig. 3: Structural View and Transverse View of Tri-Gate Transistor

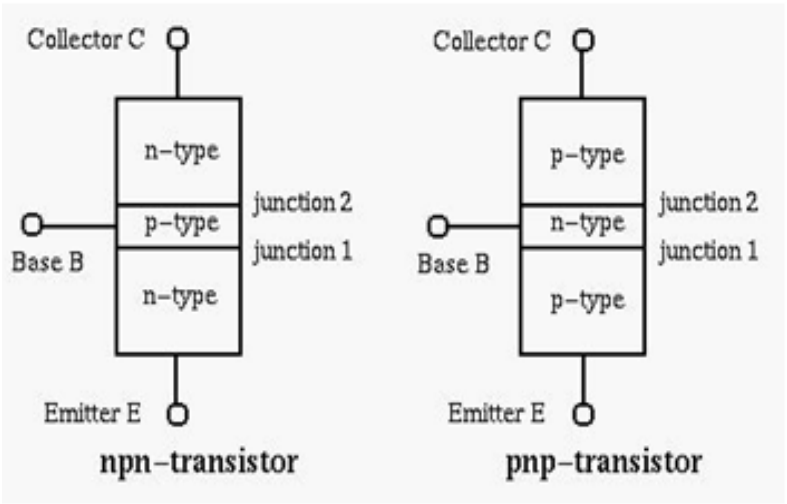

Fig. 4: Structural View of Planar Transistor

Out of these sides of transistors Side-1 is Gate-1 with height H, Side-2 acquires Gate-3 having length L, and Top side acquires Gate-3 with width W, as shown in the above figure. These transistors are manufactured either on the SOI substrate or standard mass silicon substrate.

Such designing of transistor allows three times the surface area of electrons to travel which reduce leakage and consume far less power than planar transistor which also allows up to 37% higher speed, or power consumption at fewer than 50% of current transistor as stated by Intel.

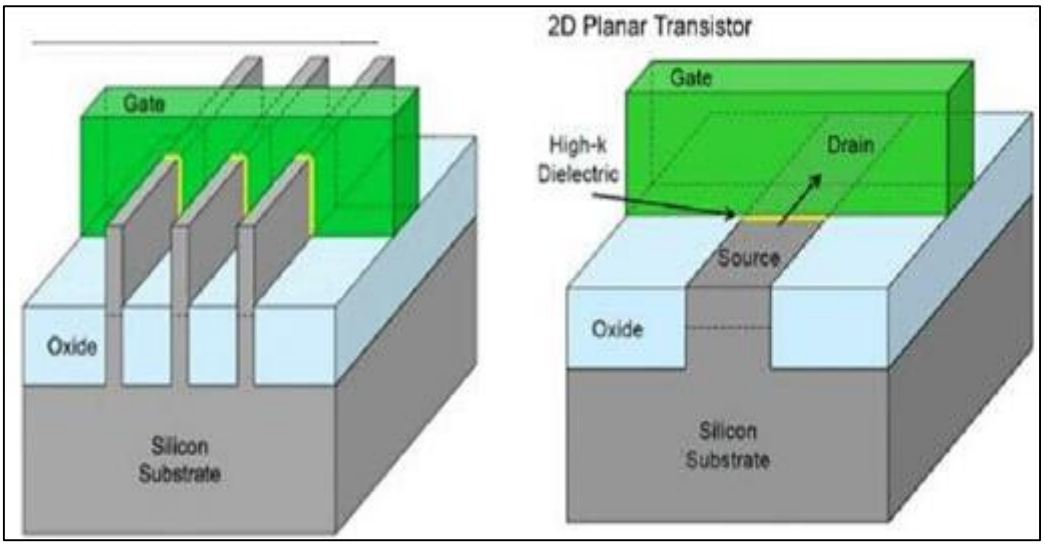

Fig. 5: Animated View of Tri-Gate Transistor vs Planar Transistor

III. SIMULATION AND TESTING

Now the question arises that how Tri-Gate Transistor is more efficient than the traditional transistor? The answer to the question is simple, its geometry itself! The Architectural design of Tri-Gate Transistor consists of three gates wrapped around the channel from source to drain, as to the traditional 2-d planar design. For the traditional planar transistor the current from drain to source is directly proportional to (W/L) ratio, also upon the oxide capacitance and mobility of carriers (majority). Equation of normal transistor is defined as –

$$I_{ds} = \left(\frac{W}{L}\right)\left(\frac{\mu C_{ox}}{2}\right)[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] \quad \ldots\ldots (1)$$

While as contrast with Tri-Gate transistor the proportionality element is expanded by 2H. Here H is width of the transistor

$$I_{ds} = \left(\frac{W+2H}{L}\right)\left(\frac{\mu C_{ox}}{2}\right)[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] \quad \ldots\ldots (2)$$

Where, I_{ds} is drain to source current
C_{ox} is oxide capacitance,
μ is mobility of electrons V_{gs} is gate to source voltage V_t is threshold voltage
Hence due to additional 2H Current characteristics will be improved and overall performance is improved.

The Simulation tests were done by Intel with other planar devices of different technologies and the test results shown in figure and Operating Voltage versus Transistor Gate Delay demonstrated as follows

IV. TRANSISTOR OPERATION

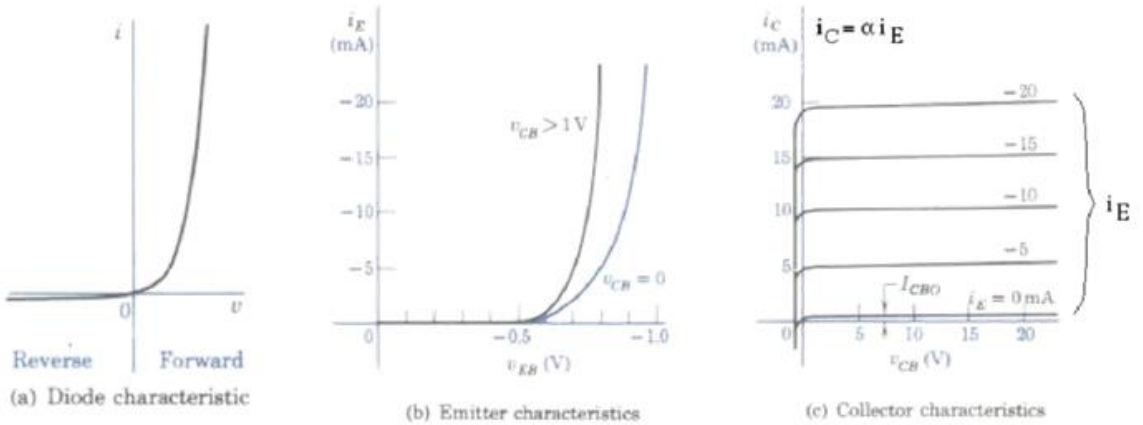

Fig. 6: Planar Transistor Characteristics

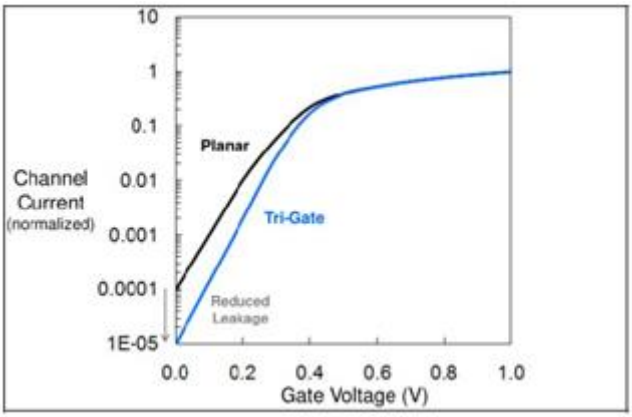

Fig. 7: The characteristics of Tri-Gate transistors provide a More extreme sub-edge slant that lessens leakage current

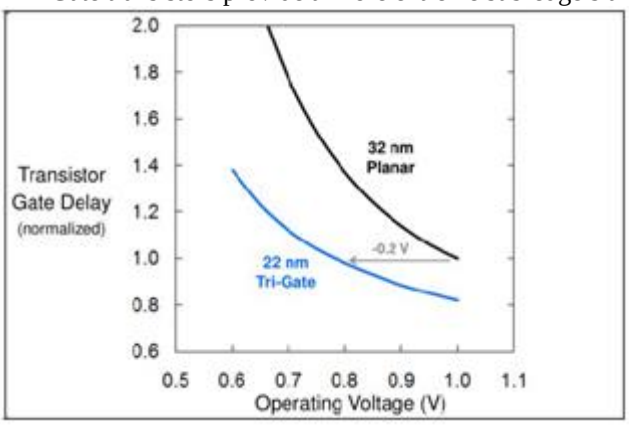

Fig. 8: 22 nm 3-D Tri-Gate transistors provide improved performance at high voltage and an unprecedented performance gain at low voltage

V. CONCLUSION

As we conclude, compared to today's traditional transistor this tri-gate transistor offers 45% of increases in speed or 50 times reduction in off-current. Also, 35% reduction in total power at constant speed. These outcomes exhibit Intel's initiative in incorporated procedures. Intel expects that these transistors could turn into the fundamental building obstructs for future microchips.

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